SERVICE MANUAL FOR

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8170 N/B MAINTENANCE

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1.Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineering specification for 8170 portable notebook computer system.

The 8170 notebook computer is a new mainstream high performance notebook in the MiTAC notebook family.

1.1.2 System Overview

CPU	mPGA 478 -PIN Socket Support Intel Pentium (Willamette)/Northwood in mFC-PGA2 package
Video	1. Dual independent Displays(LCD/CRT, LCD/TV,CRT/TV)
	2. Support Motion Compensation and iDCT
	3. Support Simultaneous display
Momory	Two 144Pin SO-DIMM ,withont and on-board Memory
PCMCIA	1. Support one slot of TypeII
	2. Non Support Zoom video/Audio Function
IDE	Support 2 IDE channel,Up to Ultra DMA 100
LCD Display	Support Dual 85MHz LVDS interface.
	Support up to QXGA(2048*1536) Resolution
Button	5 Easy Start Button(functions defined by user)& 1 Mail Receive Button
LAN	Support to 10/100 Based T
Modem	56Kbps V.90 MDC Modem
Pointing	Glide PAD with 2 Buttons and 1 scroll button
Keyboard	Internal Key Matrix Keyboard
BIOS	512KB Flash EEPROM (Include System BIOS&VGA BIOS)

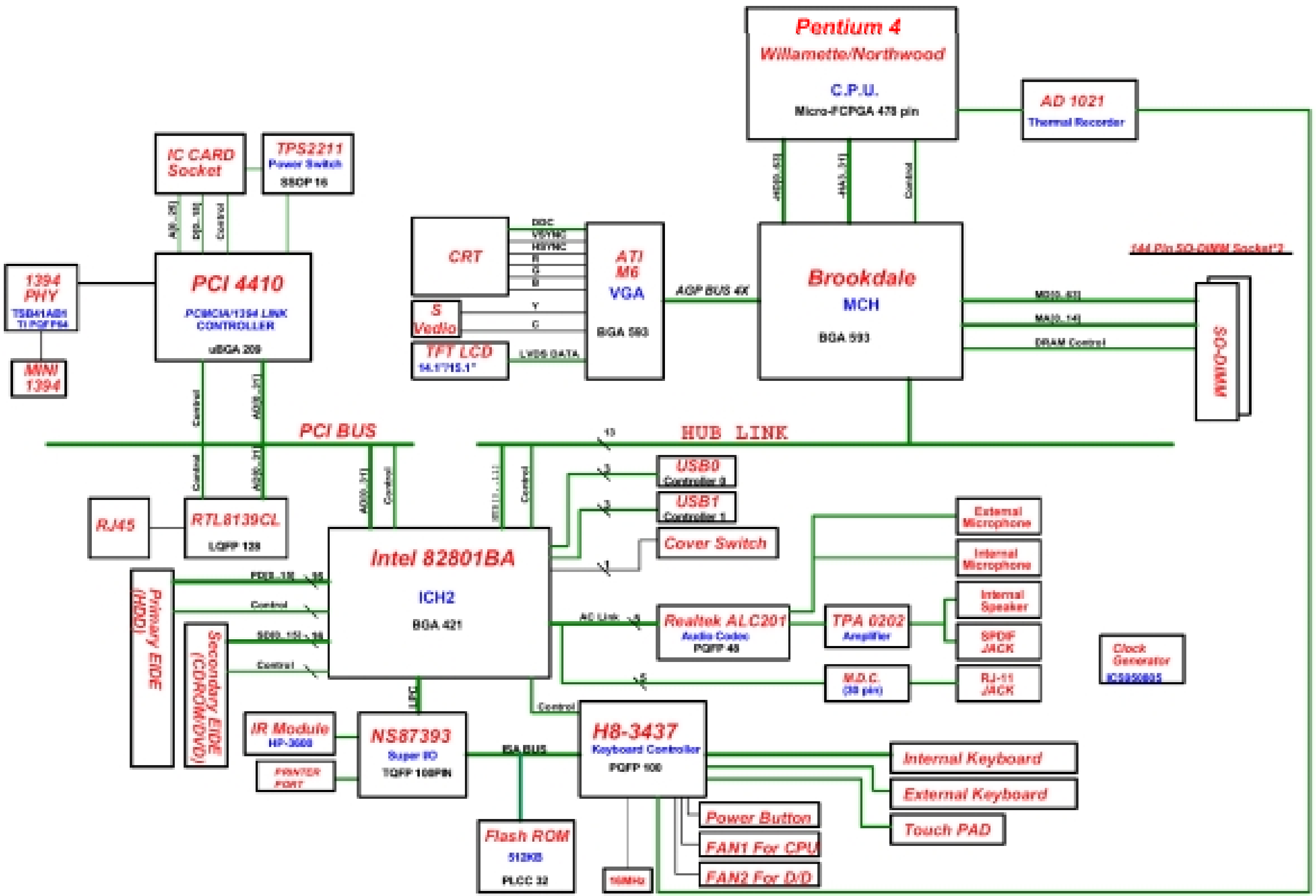
Audio	1. AC'97 Interface Codec. Sound Blaster Pro Compatible.
	2. Built-In 21W speaker and 1 Mono-Microphone
I/O Port	1. Bi-Direction Parallel Port (EPP/ECP) 2. External VGA Port(D-SUB 15Pins)
	3. 2 Standard USB 1.1 Port 4. SPIDF Jack
	5. RJ-11 Port for Modem 6. Microphone In Jck
	7. RJ-45 Port for LAN 8. VR for Audio Volume Control
	9. DC Input Jack 10.Mini IEEE 1394 Port
	11. S-Video Output Port(NTSC/PAL) 12. Battery Connector
Suspend Mode	POS(S1), Suspend to RAM(S3), Suspend to Disk(S4)
Indicator	HDD,FDD,CD-ROM,Num Lock,Caps Lock, Scroll Lock LEDs

1.2 System Architecture

1.2.1 Block Diagram(without Power System)

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8170 System Block Diagram



1.2.2 Function Description

1.2.2.1 CPU

Socket Intel Pentium 4/ Northwood processors with 100MHz FSB.400MHz system bus.Capable of mFC-PGA2 package

- Available at 1.50, 1.60, 1.70, 1.80, 1.90 and 2 GHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel® NetBurst™ micro-architecture
- System bus frequency at 400 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advance Dynamic Execution
  ---Very deep out-of-order execution
  ---Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12K micro-ops and removes decoder latency from main execution loops
- 8 KB Level 1 data cache
- 256 KB Advanced Transfer Cache (on-die,full speed Level 2 (L2) cache) with 8-way associatively and Error Correcting Code (ECC)
- 144 new Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio,encryption, and 3D performance
- Power Management capabilities
  ---System Management mode
  ---Multiple low-power states

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- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 8-way cache associatively provides improved cache hit rate on load/store operations.

1.2.2.2 CORE LOGIC

Intel Brookdale 82845 Memory Control HUB

- Intel® Pentium® 4 Processor (478 pin package) Support:
  ---Enhanced Mode Scaleable Bus Protocol
  ---2x Address, 4x Data
  ---System Bus interrupt delivery
  ---400 MHz system bus
  ---System Bus Dynamic Bus Inversion (DBI)
  ---32-bit system bus addressing
  ---12 deep In-Order Queue
  ---AGTL+ bus driver technology with integrated AGTL+ termination resistors
- System Memory Support
  ---Directly supports one SDR SDRAM channel, 64 bits wide (72 bits with ECC)
  ---133 MHz SDR SDRAM devices
  ---64 Mb, 128 Mb, 256 Mb and 512 Mb technologies for x8 and x16 devices
  ---By using 64 Mb technology, the smallest memory capacity possible is 32 MB
  ---Configurable optional ECC operation (single bit Error Correction and multiple bit Error Detection)
  ---Page sizes of 2 KB, 4 KB, 8 KB and 16 KB (individually selected for every row)
  ---Thermal management
  ---Maximum of 3 Double-Sided DIMMs (6rows populated) with unbuffered PC133 (with or without ECC)
  ---3 GB Maximum using 512 Mb technology
  ---Supports up to 24 simultaneous open pages
  ---Maximum memory bandwidth of 1.067 GB/s with PC133

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- Hub Interface to Intel® 82801BA ICH2
  ---266 MB/s point-to-point hub interface to ICH2
  ---66 MHz base clock
  ---MSI interrupt messages, power management state change, SMI, SCI and SERR error indication
- Accelerated Graphics Port (AGP) Interface
  --- Supports a single AGP device (either a connector or on the motherboard)
  ---Supports AGP 2.0 including 1x, 2x, and 4x AGP data transfers and 2x/4x Fast Write protocol
  ---Supports only 1.5 V AGP electrical characteristics
  ---32 deep AGP request queue
  ---Delayed transaction support for AGP-to-System Memory FRAME# semantic reads
- System Interrupt Support
  ---System bus interrupt delivery mechanism
  ---Interrupts signaled as upstream memory writes from AGP/PCI
  ---Supports peer MSI between hub interface and AGP
  ---Provides redirection for IPI and upstream interrupts to the system bus
- Power Management
  ---SMRAM space remapping to A0000h
  ---Supports extended SMRAM space above 256 MB, additional TSEG from Top of Memory
- interface are not supported
  ---PC ’99 suspend to DRAM support
  ---ACPI, Revision 1.0b compliant power management
  ---APM, Revision 1.2 compliant power management
  ---NT Hardware Design Guide, Version 1.0 compliant
- Package
  ---MCH: 593 pin FC-BGA (37.5 x 37.5 mm)

Intel 82801BA Internal Connect HUB

- PCI Bus I/F
  - ---Supports PCI at 33 MHz
  - ---Supports PCI Rev 2.2 Specification
  - ---133 MByte/sec maximum throughput
  - ---Supports up to 6 master devices on PCI
  - ---One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
- Integrated LAN Controller
  - ---WfM 2.0 Compliant
  - ---Interface to discrete LAN Connect component
  - ---10/100 Mbit/sec Ethernet support
  - ---1 Mbit/sec HomePNA* support
- Integrated IDE Controller
  - ---Independent timing of up to 4 drives
  - ---Ultra ATA/100/66/33, BMIDE and PIO modes
- Read transfers up to 100MB/s, Writes to 89 MB/s
  - ---Separate IDE connections for Primary and Secondary cables
  - ---Implements Write Ping-Pong Buffer for faster write performance
- USB
  - ---2 UHCI Host Controllers with a total of 4 ports
  - ---USB 1.1 compliant
  - ---Supports wake-up from sleeping states S1–S4
  - ---Supports legacy Keyboard/Mouse software
- AC'97 Link for Audio and Telephony CODECs
  - ---AC’97 2.1 compliant

---Independent bus master logic for 5 channels (PCM In/Out, Mic Input, Modem In/Out)
---Separate independent PCI functions for Audio and Modem
---Support for up to six channels of PCM audio output (full AC3 decode)
---Supports wake-up events

- Interrupt Controller
  ---Support up to 8 PCI interrupt pins
  ---Supports PCI 2.2 Message-Based Interrupts
  ---Two cascaded 82C59
  ---Integrated I/O APIC capability
  ---15 interrupts supported in 8259 mode, 24 supported in I/O APIC mode
  ---Supports Serial Interrupt Protocol
  ---Supports Front-Side Bus interrupt delivery
- 1.8 V operation with 3.3 V I/O
  ---5V tolerant buffers on IDE, PCI, USB Over current and Legacy signals
- GPIO
  ---TTL, Open-Drain, Inversion
- Timers Based on 82C54
  ---System timer, Refresh request, Speaker tone output
- Power Management Logic
  ---ACPI 1.0 compliant
  ---ACPI Power Management Timer
  ---PCI PME# support
  ---SMI# generation
  ---All registers readable/restorable for proper resume from 0V suspend states
  ---Support for APM-based legacy power management for non-ACPI implementations

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- External Glue Integration
  ---Integrated Pull-up, Pull-down and Series Termination resistors on IDE and processor interface
- Enhanced Hub I/F buffers improve routing flexibility (Not available with all Memory Controller Hubs)
- Firmware Hub (FWH) I/F supports BIOS memory size up to 8 MBs
- Low Pin count (LPC) I/F
  ---Allows connection of legacy ISA and X-Bus devices such as Super I/O
  ---Supports two Master/DMA devices.
- Enhanced DMA Controller
  ---Two cascaded 8237 DMA controllers
  ---PCI DMA: Supports PC/PCI — Includes two PC/PCI REQ#/GNT# pairs
  ---Supports LPC DMA
  ---Supports DMA Collection Buffer to provide Type-F DMA performance for all DMA channels
- Real-Time Clock
  ---256-byte battery-backed CMOS RAM
  ---Hardware implementation to indicate century rollover
- System TCO Reduction Circuits
  ---Timers to generate SMI# and Reset upon detection of system hang
  ---Timers to detect improper processor reset
  ---Integrated processor frequency strap logic
- SM Bus
  ---Host interface allows processor to communicate via SM Bus
  ---Slave interface allows an external Micro controller to access system resources
  ---Compatible with most 2-Wire components that are also I2C compatible

- Supports ISA bus via external PCI-ISA Bridge
- 360-pin EBGA package

1.2.2.3 Memory

64MB PC133 SDRAM SO-DIMM Expandable to 1024MB(2 SODIMM slots).
Support 3.3V PC133 SDR SDRAM only.

Table 1.1 *MEMORY EXPANSION CAPACITY*

Slot1	Slot2	Total
64MB	0	64MB
64MB	32MB	96MB
64MB	64MB	128MB
64MB	128MB	192MB
64MB	256MB	320MB
64MB	512MB	576MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB
256MB	256MB	512MB
256MB	512MB	768MB
512MB	512MB	1024MB

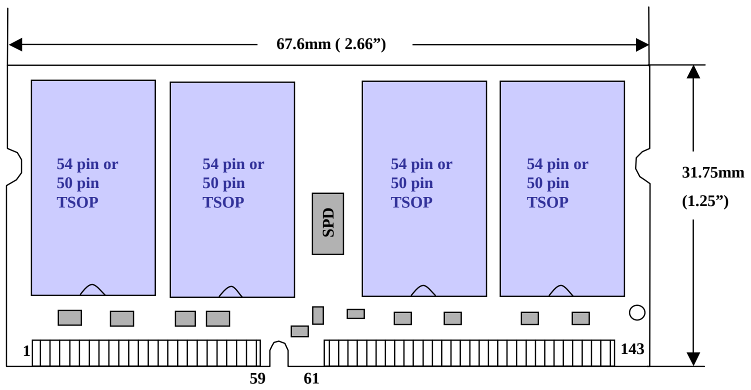


Figure 1.1 *SO-DIMM MODULE*

1.2.2.4 I/O Ports

- ***CRT Port***

@ Standard VGA compatible port

@ DDC1 and DDC2B compliant

Table 1.2 ***CRT CONNECTOR***

PIN	SIGNAL	DESCRIPTION
1	RED	Red analog video output
2	GREEN	Green analog video output
3	BLUE	Blue analog video output
4	Monitor Sense	Monitor Sense
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	Monitor Sense
12	CRT DATA	Data from DDC monitor
13	HSYNC	Horizontal Sync Control
14	VSYNC	Vertical Sync control
15	CRT CLK	Clock to DDC monitor

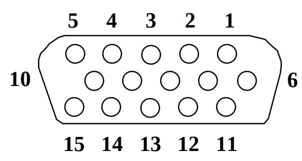


Figure 1.2 ***CRT CONNECTOR***

• ***Standard 4 Pins S-VIDEO Port for TV-Out***

@ Support 1024*768 resolution

@ Support 848*480 resolution in 16:9 mode

@ Support PAL and NTSC system

Table 1.3 *S-VIDEO CONNECTOR*

PIN	SIGNAL	DESCRIPTION
1	GND	-
2	GND	-
3	LUMA	O
4	CRMA	O

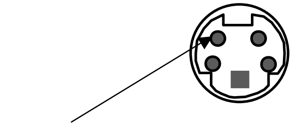


Figure1.3 *S-VIDEO Port*

• ***IEEE1394 Port***

Table 1.4 *IEEE1394 CONNECTOR*

PIN	SIGNAL	DESCRIPTION
1	TPB-	I/O
2	TPB+	I/O
3	TPA-	I/O
4	TPA+	I/O

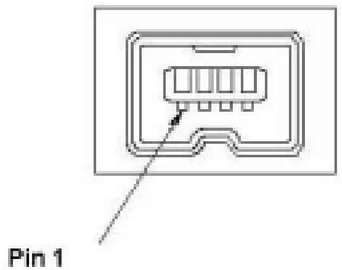


Figure1.4 *IEEE1394 Port*

• ***AUDIO Ports***

@ Built in 1 mono microphone

@ SPDIF

@ Microphone In

• ***RJ11***

@ Connection to Modem Daughter Board connector

Table 1.5 *MODEM CONNECTOR*

PIN	SIGNAL NAME	DIRECTION	DESCRIPTION
1	NC	-	No Connect
2	LINE+	I/O	Phone Line Positive
3	LINE-	I/O	Phone Line Negative
4	NC	-	No Connect

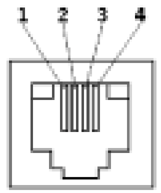


Figure 1.5 *MODEM Port*

• ***RJ45***

@ Connection to on-board NIC controller

Table 1.6 *LAN CONNECTOR*

PIN	SIGNAL NAME	DIRECTION	DESCRIPTION
1	TX+	Out	Transmit Data Ring
2	TX-	Out	Transmit Data Tip
3	RX+	IN	Receive Data Ring
4	TERM 1	-	Internal termination resistor
5	TEMR 2	-	Internal termination resistor
6	RX	IN	Receive Data Tip
7	TERM 3	-	Internal termination resistor
8	TERM 4	-	Internal termination resistor

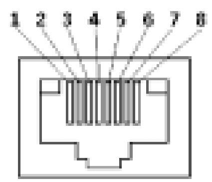


Figure 1.6 *LAN CONNECTOR*

- ***USB Port***

@ Two industry standard USB 1.1 ports

Table 1.7 *USB Port2*

PIN	SIGNAL NAME	DIRECTION	DESCRIPTION
1	VCC	-	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negaitve
3	DATA+	I/O	Balanced Data Posiitve
4	GND	-	Ground

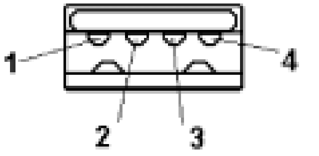


Figure 1.7 *USB Port*

- ***Parallel Port***

@ Configurable as logical ports LPT1,LPT2 or LPT3

@ EPP rev 1.7 & 1.9 compatible

@ ECP(IEEE 1284) compatible

@ Industry standard 25 Pins connector

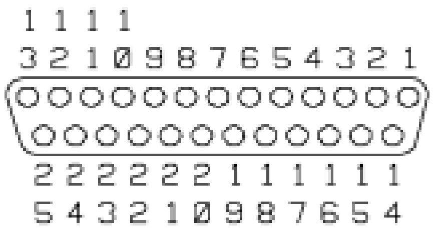


Figure 1.8 *PARALLEL PORT CONNECTOR*

Table 1.8 ***PARALLEL Port***

PIN	SIGNAL NAME	DIRECTION	DESCRIPTION
1	STROBE#	O	Data Strobe
2	PD0	I/O	PP Data bit 0
3	PD1	I/O	PP Data bit 1
4	PD2	I/O	PP Data bit 2
5	PD3	I/O	PP Data bit 3
6	PD4	I/O	PP Data bit 4
7	PD5	I/O	PP Data bit 5
8	PD6	I/O	PP Data bit 6
9	PD7	I/O	PP Data bit 7
10	-ACK	I	Printer Acknowledge
11	BUSY	I	Printer Busy
12	PE	I	Paper Out
13	SLCT	I	Print Select Acknowledge
14	-AUTOFDXT	O	Auto Line Feed
15	-ERROR	I	Printer Error
16	-INIT	O	Reset Printer
17	SLCTIN#	I	Select In
18	GND	-	Ground
19	GND	-	Ground
20	GND	-	Ground
21	GND	-	Ground
22	GND	-	Ground
23	GND	-	Ground
24	GND		Ground
25	GND	-	Ground
Case	GND	-	Ground

1.2.2.5 PC CARD SLOT

- One Type II/I slot supporting the 1997 PC Card standard, and including full R2(16-bit) and 32-bit Card bus Data transfer
- TI PCI4410(PCMXCIA Controller)& TI TPS2211(Power Switch)

1.2.2.6 GRAPHICAL SUBBSYSTEM

- ATI Mobility M6 graphical controller embedded 8M DDR SDRAM

1.2.2.7 DISPLAY

- Internal LCD Display is 14.1” TFT ISP XGA color
- External Video refresh rate of up to 100HZ support
  ---Vertical refresh frequencies to meet VESA requirements
  ---Simultaneous video in specified video modes-switchable with hot key

1.2.2.8 READ ONLY MEMORY(BIOS FLASH)

- Fully compatible with industry standard software including windows 2000 & Windows XP
- Fully support APM V1.2 and latest ACPI specification
- 4Mb Flash BIOS
- Inside BIOS core

1.2.2.9 POWER MANAGEMENT FEATURES

- Local standby mode(individual device such as HDD, graphics controller,LCD etc..)

- CPU Idle mode(including ACPI modes C1 and C2)
- Suspend mode(including S1 and S3 ACPI modes)
- Fully APM V1.2 compliant
- Fully ACPI V1.1 compliant
- Hibernate for Windows 2000 and windows XP
- Thermal management
- Fully US EPA Energy start compliant

1.2.2.10 KEYBOARD CONTROLLER

- Hitachi H8-3437S

1.2.2.11 SUPER I/O

- Ns PC87393F LPC interface Ultra I/O

1.2.2.12 LEDS INDICATOR

- CDROM & HDD & NUM & CAP & SCROLL & EMIAL

1.2.2.13 BUTTONS

- EMAIL BIN & FIVE PIECE EASY START RTN

1.2.2.14 MODEM

Table 1.9 ***MODEM DAUGHTER BOARD CONNECTOR***

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	MONO_OUT	2	NC
3	GND	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	ACSYNC
23	ACSDOUT	24	MSDIN
25	-ACRST	26	MSDIN
27	GND	28	GND
29	GND	30	ACBITCLK

1.3 Electrical Characteristic

1.3.1 Power On Sequence

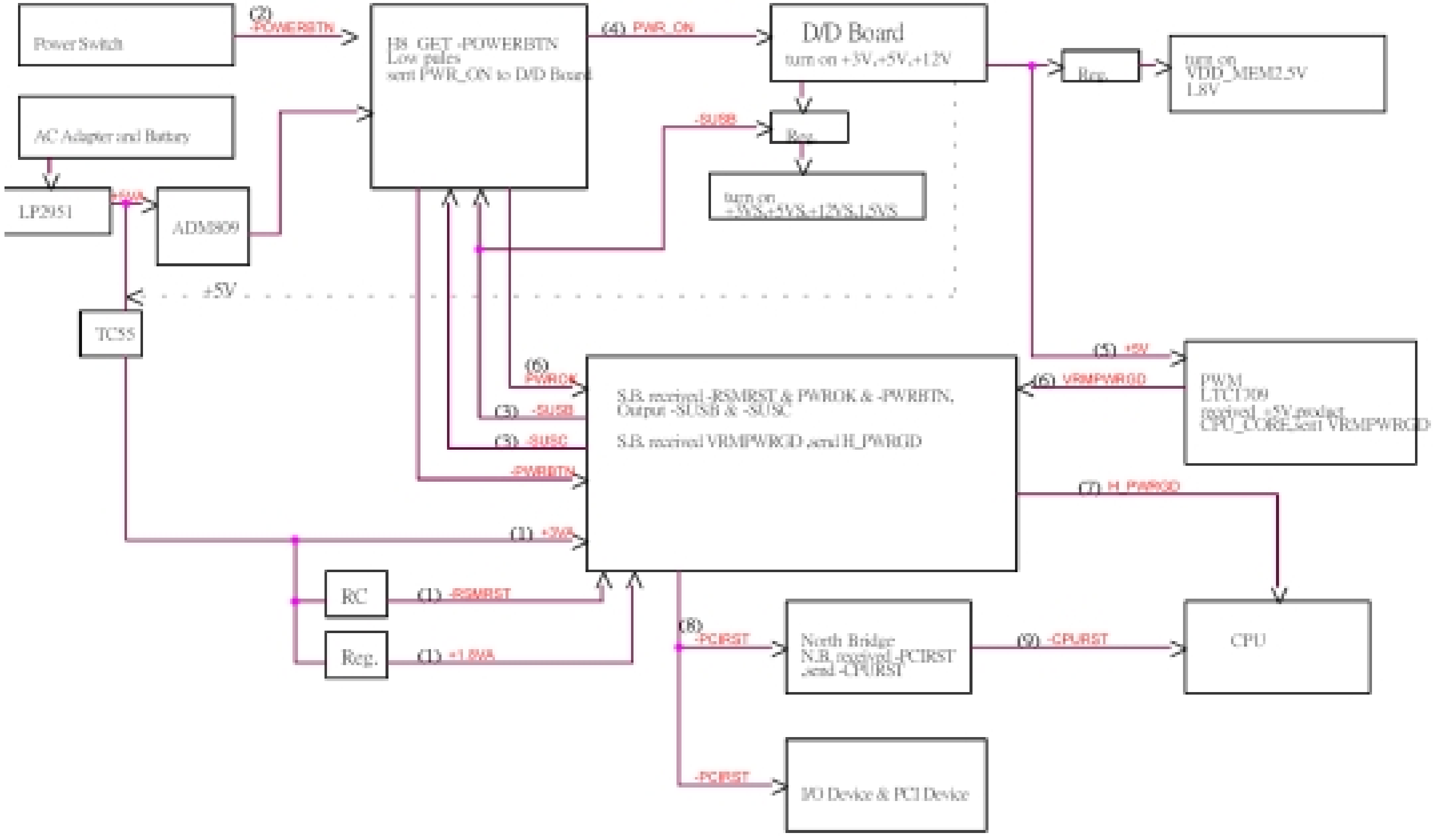


Figure 1.9 ***Power on Sequence***

1.3.2 Power On Suspend Sequence

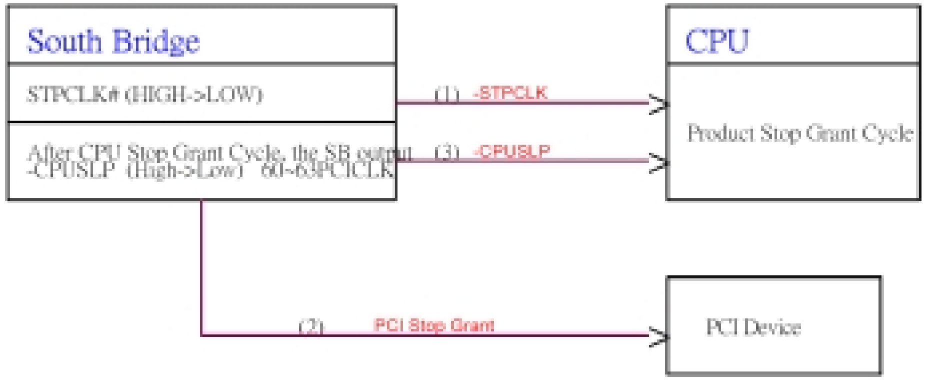


Figure 1.10 ***Power on Suspend Sequence***

1.3.3 Resume from Power Suspend Sequence

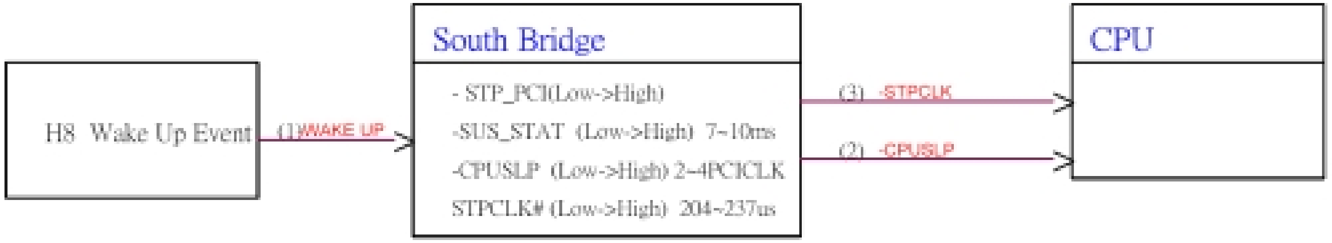


Figure 1.11 ***Resume from Power Suspend Sequence***

1.3.4 Suspend to RAM Sequence

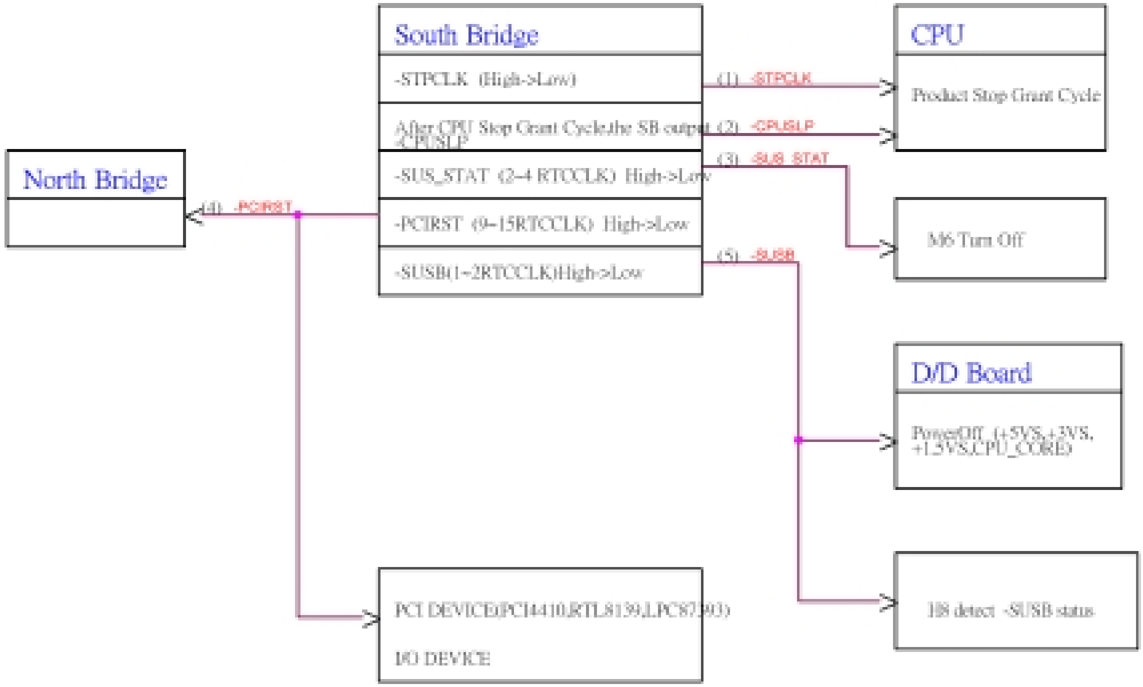


Figure 1.12 ***Suspend to RAM sequence***

1.3.5 Resume from Suspend to RAM Sequence

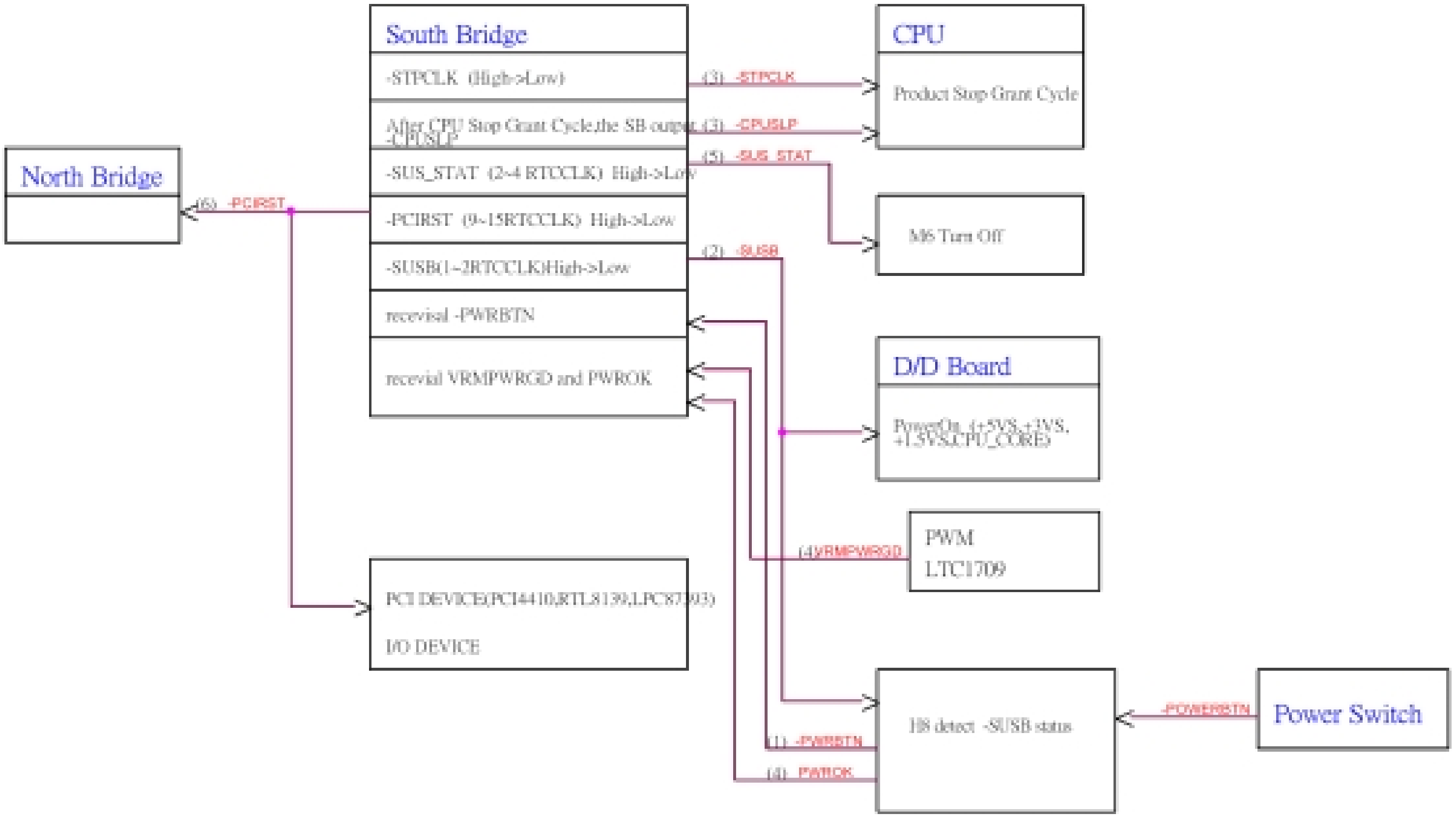


Figure 1.13 ***Resume from Suspend to RAM Sequence***

1.3.6 Suspend to Disk Sequence

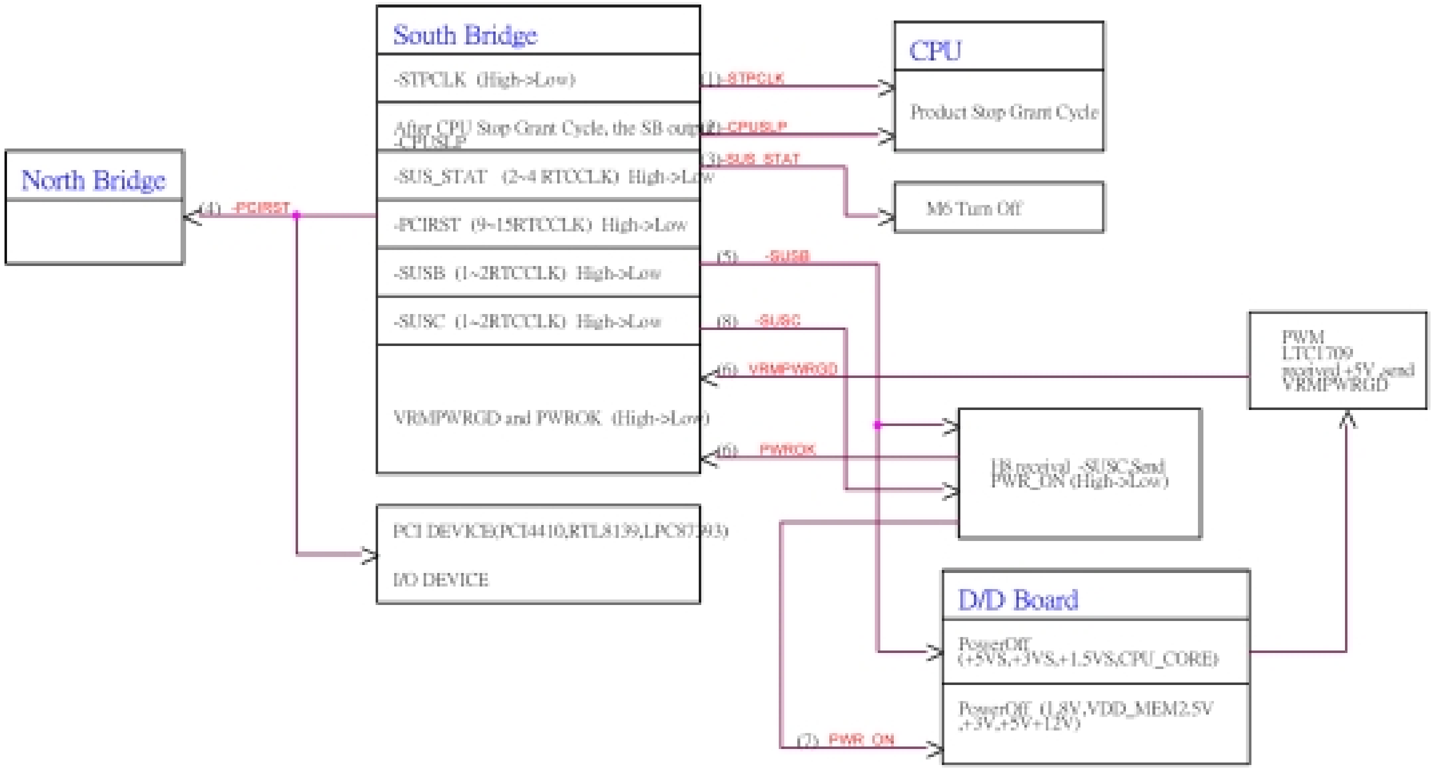


Figure 1.14 ***Suspend to Disk Sequence***

1.3.7 Resume from Suspend to Disk Sequence

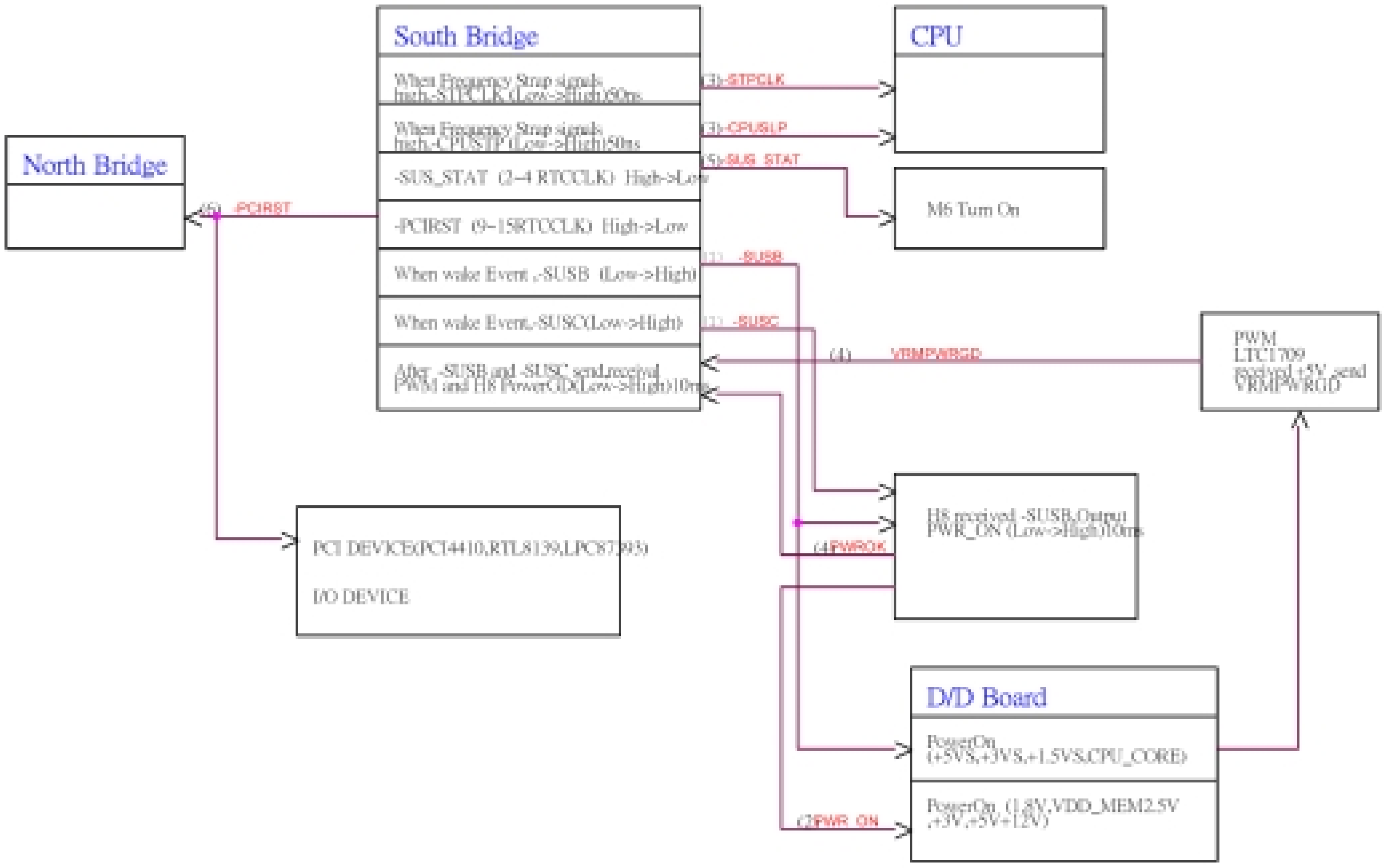


Figure 1.15 ***Resume from Suspend to Disk Sequence***

1.3.8 ICH2 GPI/O Pin Define

Pin Name	Signal Name	Power	Type	During PCIRST#	Immediately After PCIRST#	S1	S3	S4/S5	Description
GPIO0	PULL-UP	+3.3VS	I	PC/PCI DEVICE		DRIVEN			
GPIO1	PULL-UP	+3.3VS	I	PC/PCI DEVICE		DRIVEN			
GPIO2	PULL-UP	+3.3VS	X	X	X	X	X	X	X
GPIO3	PULL-UP	+3.3VS	I	HIGH-Z	HIGH-Z	HIGH-Z			
GPIO4	PULL-UP	+3.3VS	I	HIGH-Z	HIGH-Z	HIGH-Z			
GPIO6	PULL-UP	+3.3VS	I	MAIN I/O					
GPIO7	PULL-UP	+3.3VS	I						
GPIO8	-SCI	+3.3VA	I						ACPIMODE-SCI
GPIO11	PULL-UP	+3.3VA	I	HIGH-Z	HIGH-Z	DEFINED	DEFINED	DEFINED	
GPIO12	-EXTSMI	+3.3VA	I						DOS MODE -SMI
GPIO13	PULL-UP	+3.3VA	I						
GPIO16	TP	+3.3VS	O	HIGH-Z	HI	HI	OFF	OFF	
GPIO17	PULL-UP	+3.3VS	O	HIGH-Z	HI	HI	OFF	OFF	
GPIO18	PULL-UP	+3.3VS	O	HI		DEFINED	OFF	OFF	
GPIO19	-ENABKL_MASK	+3.3VS	O	HI	HI	DEFINED	OFF	OFF	MASK ENABLE
GPIO20	-CDROM_PWRON	+3.3VS	O	HI	HI	DEFINED	OFF	OFF	Control CDROM Power on
GPIO21	-HDD_PWRON	+3.3VS	O	HI	HI	DEFINED	OFF	OFF	Control HDD Power on
GPIO22	DRAMENA	+3.3VS	O	HIGH-Z	HIGH-Z	DEFINED	OFF	OFF	DRAM Data select
GPIO23	PULL-UP	+3.3VS	OD	LOW	LOW	DEFINED	OFF	OFF	
GPIO24	-1394WR	+3.3VA	O	HIGH-Z	HI	DEFINED	DEFINED	DEFINED	1394EEPROM R/W
GPIO25	-PCIRST_MSK	+3.3VA	O	HIGH-Z	HI	DEFINED	DEFINED	DEFINED	MASK PCIRST
GPIO27	-GATE1394	+3.3VA	O	HIGH-Z	HI	DEFINED	DEFINED	DEFINED	RST CARD BOARD
GPIO28	SPK_OFF	+3.3VA	O	HIGH-Z	HI	DEFINED	DEFINED	DEFINED	OFF SPEAKER

1.3.9 Power Consumption Of Suspend Mode

- Suspend To RAM<TBD
- Suspend To Disk/Soft-Off/Mechanical Off<TBD

1.3.10 Clock Harmonic List

Clock Harmonic Unit: M														
	12.288	14.318	16	24	24.576	25	27	32.758	33	48	65	66	100	133
1	12.288	14.318	16	24	24.576	25	27	32.758	33	48	65	66	100	133
2	24.576	28.636	32	48	49.152	50	54	65.516	66	96	130	132	200	266
3	36.864	42.954	48	72	73.728	75	81	98.274	99	144	195	198	300	399
4	49.152	57.272	64	96	98.304	100	108	131.032	132	192	260	264	400	532
5	61.44	71.59	80	120	122.88	125	135	163.79	165	240	325	330	500	665
6	73.728	85.908	96	144	147.456	150	162	196.548	198	288	390	396	600	798
7	86.016	100.226	112	168	172.032	175	189	229.306	231	336	455	462	700	931
8	98.304	114.544	128	192	196.608	200	216	262.064	264	384	520	528	800	1064
9	110.592	128.862	144	216	221.184	225	243	294.822	297	432	585	594	900	1197
10	122.88	143.18	160	240	245.76	250	270	327.58	330	480	650	660	1000	1330
11	135.168	157.498	176	264	270.336	275	297	360.338	363	528	715	726	1100	1463
12	147.456	171.816	192	288	294.912	300	324	393.096	396	576	780	792	1200	1596
13	159.744	186.134	208	312	319.488	325	351	425.854	429	624	845	858	1300	1729
14	172.032	200.452	224	336	344.064	350	378	458.612	462	672	910	924	1400	1862
15	184.32	214.77	240	360	368.64	375	405	491.37	495	720	975	990	1500	1995
16	196.608	229.088	256	384	393.216	400	432	524.128	528	768	1040	1056	1600	2128
17	208.896	243.406	272	408	417.792	425	459	556.886	561	816	1105	1122	1700	2261
18	221.184	257.724	288	432	442.368	450	486	589.644	594	864	1170	1188	1800	2394
19	233.472	272.042	304	456	466.944	475	513	622.402	627	912	1235	1254	1900	2527
20	245.76	286.36	320	480	491.52	500	540	655.16	660	960	1300	1320	2000	2660
21	258.048	300.678	336	504	516.096	525	567	687.918	693	1008	1365	1386	2100	2793
22	270.336	314.996	352	528	540.672	550	594	720.676	726	1056	1430	1452	2200	2926
23	282.624	329.314	368	552	565.248	575	621	753.434	759	1104	1495	1518	2300	3059
24	294.912	343.632	384	576	589.824	600	648	786.192	792	1152	1560	1584	2400	3192
25	307.2	357.95	400	600	614.4	625	675	818.95	825	1200	1625	1650	2500	3325

26	319.488	372.268	416	624	638.976	650	702	851.708	858	1248	1690	1716	2600	3458
27	331.776	386.586	432	648	663.552	675	729	884.466	891	1296	1755	1782	2700	3591
28	344.064	400.904	448	672	688.128	700	756	917.224	924	1344	1820	1848	2800	3724
29	356.352	415.222	464	696	712.704	725	783	949.982	957	1392	1885	1914	2900	3857
30	368.64	429.54	480	720	737.28	750	810	982.74	990	1440	1950	1980	3000	3990
31	380.928	443.858	496	744	761.856	775	837	1015.5	1023	1488	2015	2046	3100	4123
32	393.216	458.176	512	768	786.432	800	864	1048.26	1056	1536	2080	2112	3200	4256
33	405.504	472.494	528	792	811.008	825	891	1081.01	1089	1584	2145	2178	3300	4389
34	417.792	486.812	544	816	835.584	850	918	1113.77	1122	1632	2210	2244	3400	4522
35	430.08	501.13	560	840	860.16	875	945	1146.53	1155	1680	2275	2310	3500	4655
36	442.368	515.448	576	864	884.736	900	972	1179.29	1188	1728	2340	2376	3600	4788
37	454.656	529.766	592	888	909.312	925	999	1212.05	1221	1776	2405	2442	3700	4921
38	466.944	544.084	608	912	933.888	950	1026	1244.8	1254	1824	2470	2508	3800	5054
39	479.232	558.402	624	936	958.464	975	1053	1277.56	1287	1872	2535	2574	3900	5187
40	491.52	572.72	640	960	983.04	1000	1080	1310.32	1320	1920	2600	2640	4000	5320

1.3.11 Audio Performance

- 8170 meet all the following items.

Table 1.10 *Digital Playback (PC-D-A) for line Output*

Test Items	Mobile System
Full Scale Output Voltage	>=0.7Vrms(3.3V audio)
Sample Frequency Accuracy	<=0.1
Frequency Response(44.1ks/sec)	20Hz~15Hz
Frequency Response(48ks/sec)	20Hz~15Hz
Dynamic Range(SNR)	>=70dBFSA
THD+N	<=-55dBFS
Cross-talk	>=50dB

Table 1.11 ***Analog Pass-Through(A-A) for line input to line Output***

Test Items	Mobile System
Frequency Response	20Hz~15kHz
Dynamic Range(SNR)	>=70dBFSA
THD+N	<=-55dBFS
Cross-talk	>=50dB

Table 1.12 ***Analog Pass-Through(A-A) for Microphone input to line Output***

Test Items	Mobile System
Frequency Response	100Hz~12kHz
Dynamic Range(SNR)	>=60dBFSA
THD+N	<=-50dBFS

Table 1.13 ***Digital Recording(A-D-PC) for Microphone input***

Test Items	Mobile System
Full Scale Input Voltage	>=100mVrms
Sample Frequency Accuracy	<=0.1%
Frequency Response(22.05ks/sec)	100Hz~8.8kHz
Dynamic Range(SNR)	>=60dBFSA
THD+N	<=-50dBFS

1.4 APPENDIX

APPENDIX A WILLAMETTE CPU CORE FEQUENCY SELECTION

Bus Ratio	Core Freq	LINT[1]#NMI	A20M#	IGNNE#	LINT[0]#/INTR
1/8	800MHz	H	H	H	H
1/10	1.00GHz	H	H	L	H
1/11	1.10GHz	H	H	L	L
1/12	1.2GHz	H	L	H	H
1/13	1.3GHz	H	L	H	L
1/14	1.4GHz	H	L	L	H
1/15	1.5GHz	H	L	L	L
1/16	1.6GHz	L	H	H	H
1/17	1.7GHz	L	H	H	L
1/18	1.8GHz	L	H	L	H
1/19	1.9GHz	L	H	L	L
1/20	2.0GHz	L	L	H	H
1/21	2.1GHz	L	L	H	L
1/22	2.2GHz	L	L	L	H
1/23	2.3GHz	H	H	H	L
1/24	2.4GHz	L	L	L	L

APPENDIX B VOLTAGE INDENTIFICATION DEFFINITION

VID4	VID3	VID2	VID1	VID0	Vcc_max
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

APPENDIX C FREQUENCY TABLE FOR BCLK[1:0]

BSEL1	BSEL0	Function
L	L	100MHZ
L	H	RSV
H	L	RSV
H	H	RSV

LCD CABLE REQUIREMENT

- Each differential pair need meet maximum in impedance 100Ω
- DC impedance have to meet maximum impedance 5m Ω in each line

Unipac UB 141X01/Hyundai HT14X13/HannStar HSD141PX11 LCD Cable Pin Define

Signal name	M/B Pin Number	LCD module pin number
LCDVCC	1	1
LCDVCC	2	2
GND	3	3
GND	4	4
GND	5	7
GND	6	10
TX2CLK+	7	NC
TXCLK+	8	15
TX2CLK-	9	NC
TRCLK-	10	14
GND	11	13
GND	12	16

TX2OUT0+	13	NC
TX2OUT1+	14	NC
TX2OUT0-	15	NC
TX2OUT1-	16	NC
GND	17	NC
GND	18	NC
TX2OUT2+	19	NC
TXOUT0+	20	6
TX2OUT2-	21	NC
TXOUT0-	22	5
GND	23	19
GND	24	20
TXOUT2+	25	12
TXOUT1+	26	9
TXOUT2-	27	11
TXOUT1-	28	8
GND	29	NC
GND	30	NC
LCD_ID0	31	NC
+3VS	32	NC
LCD_ID1	33	NC
+3VS	34	NC
LCD_ID2	35	NC
+3VS	36	NC
NC	37	NC
NC	38	NC
NC	39	NC
NC	40	NC

LCD Panel Type	Link Pin
Unipac 14.1" TFT:UB 141X01	31&32 tied together
Hyundai 14.1" TFT: HT14X13	33&34 tied together
HannStar 14.1" TFT: HSD141PX11	31&32,33&34 tied together

COM N141P1 LCD Cable Pin Define

Signal name	M/B pin Number	LCD module pin number
LCDVCC	1	1
LCDVCC	2	2
GND	3	3
GND	4	4
GND	5	NC
GND	6	NC
TX2CLK+	7	20
TXCLK+	8	12
TX2CLK-	9	19
TXCLK-	10	11
GND	11	NC
GND	12	NC
TX2OUT0+	13	14
TX2OUT1+	14	16
TX2OUT0-	15	13
TX2OUT1-	16	15
GND	17	NC
GND	18	NC
TX2OUT2+	19	18

TXOUT+	20	6
TX2OUT2-	21	17
TXOUT0-	22	5
GND	23	NC
GND	24	NC
TXOUT2+	25	10
TXOUT1+	26	8
TXOUT2-	27	9
TXOUT1-	28	7
GND	29	NC
GND	30	NC
LCD_ID0	31	NC
+3VS	32	NC
LCD_ID1	33	NC
+3VS	34	NC
LCD_ID2	35	NC
+3VS	36	NC
NC	37	NC
NC	38	NC
NC	39	NC
NC	40	NC

DISPLAY	Link Pin
COM 14.1" SXGA+N141P1	35&36 tied together

LCD Panel ID Define Table

LCD Panel	LCD_ID2	LCD_ID1	LCD_ID0
Uniqac	0	0	1
Hyundai	0	1	0
HannStar	0	1	1
CMO	1	0	0

1.5 BIOS Specification

1.5.1 BIOS Feature

@ Inside BIOS for Intel 845 + ICH2 chipset

@ 256KB flash ROM

@ ACPI 1.0b Compliant (S1, S3, S4, S4BIOS)

@ Support APM 1.2 (POS, STR, STD)

@ SMBIOS 2.3.1

@ Support external 1.44MB USB Floppy

@ Support DVD-ROM and CD-ROM

@ Support Multi-boot function

@ Plug & Play for Devices

@ Support FIR

@ Silence Boot with Logo customized

@ Wake-up from USB

@ Fast boot bypass RAM/Floppy/CDROM testing

@ BIOS Lock function
Add the BIOS lock string at shadow memory address F000:E0C2

1.5.2 Component&Drives

Please refer to the chapter of Power Management for state definitions. For PCI and PnP terms, please refer to respective specifications

1.5.2.1 CPU

@ Intel Pentium 4 Processors Willamette//Northwood, Support upto 1.7GHz, 400 Mhz FSB

@ Pentium 4 with 256K L2 Cache

@ 64Kbyte on-chip L1 Cache

@ CPU's Power transition (Please refer to the chapter of Power Management for state definitions)
When in G0/Full-On, CPU can be in C0/C1/C2.
When in G1(STR)/G2(STD)/G3(Mechanical Off) State, CPU power is removed.

1.5.2.2 Memory System

@ Two SODIMM for SDRAM extension from 64MB to 512MB Pentium 4 with 256K L2 Cache

@ 400MHz Host Bus, 33MHz PCI Bus, 133MHz Memory Clock

@ Dynamically row power-down

@ Support Auto-refresh and Self-refresh command

@ Auto-detect CAS latency Programming

@ Memory Auto-sizing

@ 1/2/4 Bank SDRAM support, up to 4 page could open at any time

1.5.2.3 PCI Devices

@ **USB**

---4 USB port are built in SB chipset (only 2 are supported in this model)

---Wake up from USB device is supported on POS/STR

@ **VGA**

---LCD panel could be turn on/off via function hotkey, or Lid switch if users define "Blank LCD" on cover closed in SCU.

---When in G0/Full-On/Idle, VGA stays in D0 state, Panel stays on. However, if no VGA activities detected for a specific period defined in SCU, VGA will go to D1 state, and Panel will be turned off.

---When in G2/G3/STD/Soft-Off/Mechanical Off State, VGA and Panel are power off.

---When in G1/Standby, VGA stays in D2 state, Panel stays off, Hsync/Vsync is cut.

---When in G1/STR, VGA stays in D3 state, Panel stays off, Hsync/Vsync is cut, especially, Note: VRAM is shared on system DRAM, so no special circuit is provided for VRAM refresh when G1/STR.

@ **AUDIO**

---When in G0/Full-On/Idle, Audio stays in D0 state

---When in G2/G3/STD/Soft-Off/Mechanical Off State, Audio is power off.

@ **MODEM**

---Ring wake-up supported in G1/Standby/Suspend states.

---When in G0/Full-On/Idle, Modem stays in D0 state

---When in G2/G3/STD/Soft-Off/Mechanical Off State, Modem is power off.

@ **PMCIA(TI4410)**

---PME# supported

---Ring wake-up supported in G1/Standby/Suspend states.

---When in G0/Full-On/Idle, PCMCIA stays in D0 state if PC card is inserted, and stays in D2 state once PC card is removed.

---When in G2/G3/STD/Soft-Off/Mechanical Off State, PCMCIA is power off.

---When in G1/Standby, PCMCIA stays in D1 state.

---When in G1/Suspend, PCMCIA stays in D3 state.

@ **IEE1394(TI4410)**

--- PME# supported

@ **LAN(RTL8139CL)**

---PME# supported

---Ring wake-up supported in G1/Standby/Suspend states.

PCI Devices IDSEL

PCI Device	IDESL	Register Setting	Bus/ Device/ Function
Intel 845			00 / 00 / 00
P2P (NB)			00 / 01 / 00
P2P (SB)	AD14		00 / 30 / 00
LPC Bridge	AD15		00 / 31 / 00
IDE	AD15		00 / 31 / 01
USB #1	AD15		00 / 31 / 02
SMB	AD15		00 / 31 / 03
USB #2	AD15		00 / 31 / 04
AC'97	AD15		00 / 31 / 05
MC'97	AD15		00 / 31 / 06
VGA			01 / 00 / 00
LAN	AD18		02 / 02 / 00
PCMCIA	AD19		02/ 03 / 00
IEEE 1394	AD19		02/ 03 / 01

PCI IRQ Routing

CI Device	PIRQ A	PIRQ B	PIRQ C	PIRQ D	PIRQ H	PFA	Bus/ Device/ Function
Intel 845						0x0000	00 / 00 / 00
P2P (NB)						0x0008	00 / 01 / 00
P2P (SB)						0x00F0	00 / 30 / 00
LPC Bridge						0x00F8	00 / 31 / 00
IDE						0x00F9	00 / 31 / 01
USB #1				INT D#		0x00FA	00 / 31 / 02
SMB						0x00FB	00 / 31 / 03
USB #2					INT C#	0x00FC	00 / 31 / 04
AC'97		INT B#				0x00FD	00 / 31 / 05
MC'97		INT B#				0x00FE	00 / 31 / 06
VGA	INT A#					0x0100	01 / 00 / 00
LAN					INT A#	0x0210	02 / 02 / 00
PCMCIA	INT A#					0x0218	02/ 03 / 00
IEEE 1394			INT B#			0x0219	02/ 03 / 01

1.5.2.4 PCI Device

@ **Plug & Play Interface**

---Plug and Play BIOS Spec. Rev. 1.0A Compliant

---No ESCD supported

@ **RTC**

---User could setup current date and time in SCU. RTC must be Y2K compliant

---User could also setup a RTC wake-up event at any time of a month.

@ **DMA**

---ECP/FIR also use DMA but they are programmable

@ **PIC**

---IRQ0 is used by the system timer

---IRQ1 is used by KBC (Key Board Controller)

---IRQ2 is used by slave PIC

---IRQ3 is used by IR

---IRQ5 is used by Audio

---IRQ7 is used by LPT port

---IRQ8 is used by RTC (Real Time Clock)

---IRQ9 is shared by SCI

---IRQ10 is used by LAN

---IRQ10 is used by PCMCIA

---IRQ10 is used by IEEE 1394

---IRQ10 is also shared by VGA

---IRQ12 is used by mouse

---IRQ13 is used internally by CPU to recognize FPU interrupts

---IRQ14 is used by IDE channel 1

---IRQ15 is used by IDE channel 2

---Preserve two IRQs (4, 6, 11) for other devices to use.

@ **Super I/O**

---SIO chip could enter a full power down mode once system enter Suspend states

---Printer Port
Print port will enter power down mode when G1/G2/G3/STD/Suspend/Standby state.

---IR Port
IR port will enter power down mode and IR module's power will be cut off when G1/G2/G3/STD/ Suspend/Standby state.

@ **KBC**

---H8 will automatically control its power state. Please refer to KBC's specification

1.5.2.5 IDE Devices

@ **Hard Disk**

---HD will enter standby mode whenever no access request is made.

---HD will enter standby mode when the system entering Standby state.

---HD will enter sleep mode when the system entering Suspend state.

@ **CDROM**

---CD drive will enter standby mode whenever no access request is made.

---CD drive enter standby mode when the system entering Standby state.

---CD drive enter sleep mode when the system entering Suspend state

1.5.2.6 AC’97 Device

@ **AC’97 Interface**

@ **Audio Codec**

---Enter the most power saving state during Suspend.

@ **Modem Codec**

---Enter the most power saving state during Suspend

1.5.2.7 SMB

(1) **South Bridge SMB BUS**

@ **SMBUS Device**

SMB Device	Read Addr	Write Addr
SDRAM 0	0xA1	0xA0
SDRAM 1	0xA1	0xA0
CLK_GEN	0xD3	0xD2

@ **SDRAM**

---Use SMB link to read configuration data from SDRAM

---Turn off clock if no SO-DIMM insert automatically when POST

@ **Clock Generator**

---Spread spectrum is enabled during POST

(2) **H8 SMB BUS**

@ **Battery Pack**

---This is polling by KBC (H8)

@ **Thermal Sensor**

---Sensed by H8

@ **Charger**

---Directly controlled by H8, please refer to KBC specification

1.5.2.8 Mechanics

@ **Button**

---1 Power Button, 5 Easy Start Buttons, 1 E-Mail Received Button.

@ **LID Switch**

---See 1.6.7

@ **LEDs**

---All LEDs are controller via H8, Please refer to H8 Specification

@ **FAN**

---Controlled by H8

1.5.3 BIOS Setup

1.5.3.1 Introduction

SCU allows you to configure the BIOS settings. Those settings are vital for your notebook to identify the types of installed devices as well as to utilize special features. Typical menu items include Date and Time, the types of disk drives, and IDE settings. Special features include Power Saving and Password settings

The settings information is stored in the CMOS (Complementary Metal Oxide Semiconductor) RAM, which is powered by a RTC backup battery.

You may need to run SCU when

* You see an error message on the screen requesting you to run SCU
* You want to restore the factory default settings
* You want to modify some specific settings

1.5.3.2 Starting SCU

SCU is built into the system board. To run SCU, press [F2] during system startup. The main SCU screen appears as shown in Figure 1.15.

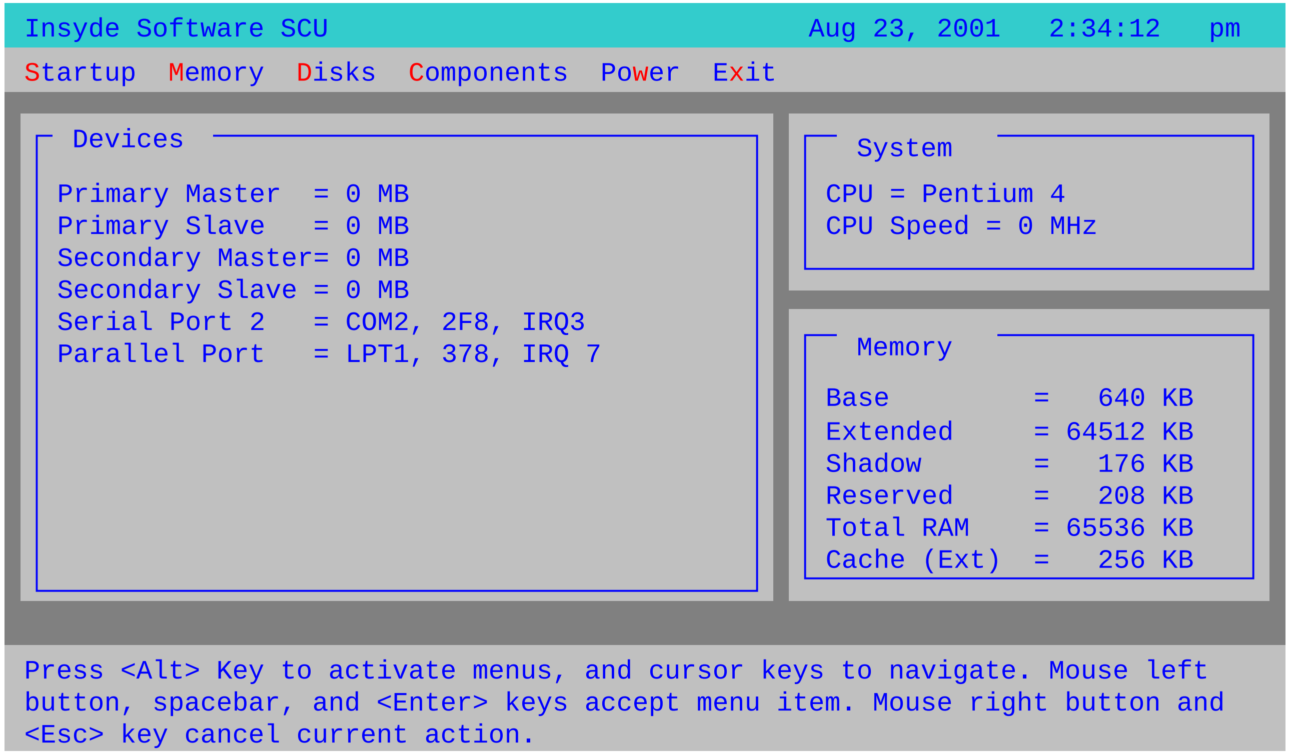


Figure 1.16 ***Main SCU Screen***

The SCU screen can be divided into three areas:

@ On the top line of the screen is the menu bar, which lists the titles of the available menus Each menu title contains a pull-down menu, which displays items for settings

@ The middle section of the screen displays current settings of the system. If you open a pull-down menu and select an item that provides multiple options, a submenu will pop up and let you make further selections.

@ The bottom window provides alternative information. Normally it gives the keyboard/mouse instructions for moving around and making selections. When a menu item is highlighted, the window will provide more detailed description of the item.

1.5.3.3 Moving Around and Making Selections

You must go through two or three levels to complete the setting for an item. In most cases, there are three levels: menu title, pull-down menu, and submenu.
To move around and make selections, you can use both the touch pad/mouse and keyboard

@ **Using the Touch pad/Mouse**
You are advised to use the touch pad or mouse. It is more straightforward than using the keyboard.
For most items, simply move the pointer with the touch pad/mouse and left-click on the intended item.
To cancel your selection, click the right button. For some items, you will need to select with the arrow keys.

@ **Using the keyboard**
Keyboard information can be found at the bottom of the screen. You can also use the shortcut key, which is highlighted in a different color on the screen.

Described below is the general procedure to complete a setting by use of the keyboard:

® Select a menu title with the left/right arrow key and press [Enter] to pull down the menu. You can directly pull down a menu You can directly pull down a menu by pressing [Alt] and the shortcut key.

® From the pull-down menu, select an item with the up/down arrow key and press [Enter] to access the submenu or change the setting, The submenu displays further options that you can select.

® For most menu items, pressing the [Tab] key will jump from one item to another, thus allowing you to go through the items quickly. To confirm the changes you make, press [Enter] or select the OK button. To cancel the changes, press [Esc] or select the Cancel button.

1.5.3.4 Startup Menu

The Startup pull-down menu, as shown below, contains some basic configuration and password settings of the system

Startup

```
   Date and Time              >
   Splash Boot Logo
 √ Fast Boot
   Boot Device                >
   Set Admin password         >
   Set User password          >
   SCU Color Scheme           >
```

@ **Data and time**

The "Date and Time" item sets the system date and time. When this item is selected, the submenu will display as shown below:

```
          Date and Time

  Day          23    Hour      16
  Month         8    Minute    56
  Year       2001    Second    53

         OK          Cancel
```

@ Splash Boot Logo

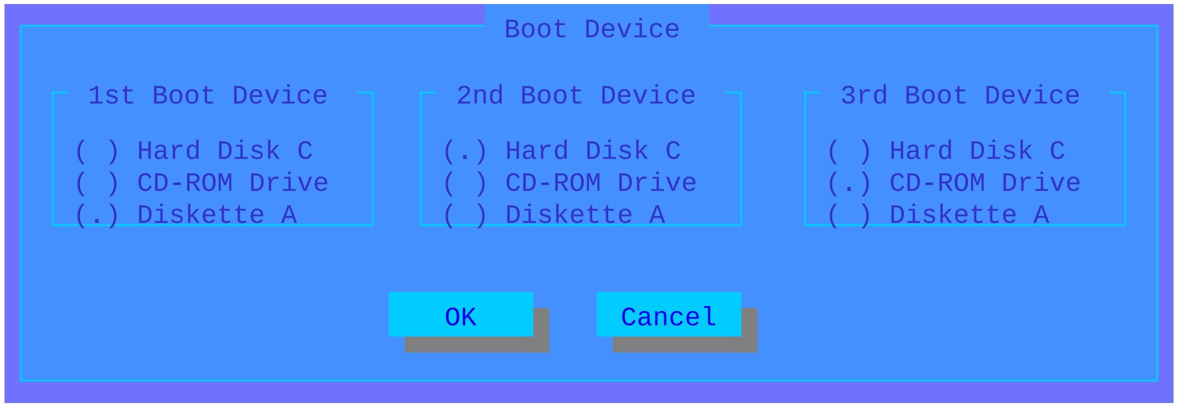
The "Splach boot Logo" item to enable or disable the big boot logo on screen when system is booting. When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates Disabled. The default setting is Disabled

@ Fast Boot

The "Fast Boot" item, when enabled, speeds up the booting procedure by bypassing the memory test. When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates Disabled. The default setting is Enabled.

@ Boot Device

The "Boot Device" item sets the sequence of booting device. When this item is selected, the submenu will display as shown below.

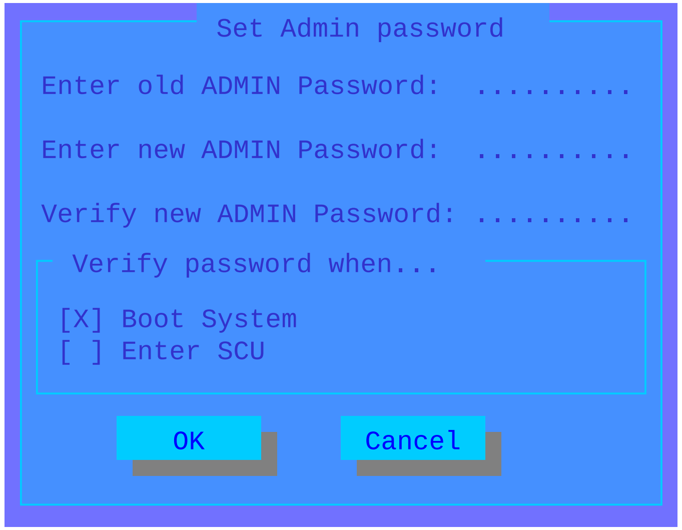


The default setting is Diskette A, Hard Disk C, then CD-ROM Drive

❖ **NOTE:** If you set all booting options to the same device (say, Hard Disk C),. then the notebook will try to boot from that device only

@ Set Admin Password

This item lets you set up administrator-level password. When this item is selected, the submenu will display as shown below:



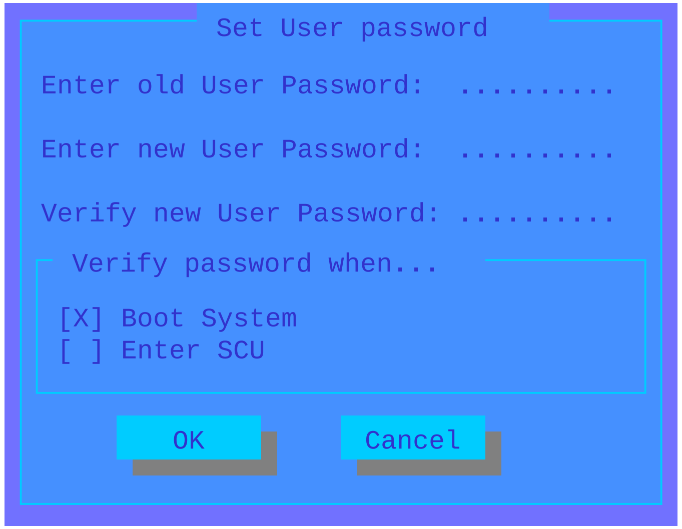
You can directly enter the new password if no password has previously existed. If a password has been previously set up, you have to enter the correct old password before setting up a new one. In either case, you have to enter the new password twice to complete the setting.

❖ **NOTE:**

1. If you want to clear a previous password, you can enter the old password and leave the following fields blank
2. The administrator password is required for booting and entering SCU, so the "Verify password when …" setting can not be changed

@ Set User Password

This item lets you set up user-level password. When this item is selected, the submenu will display as shown below:



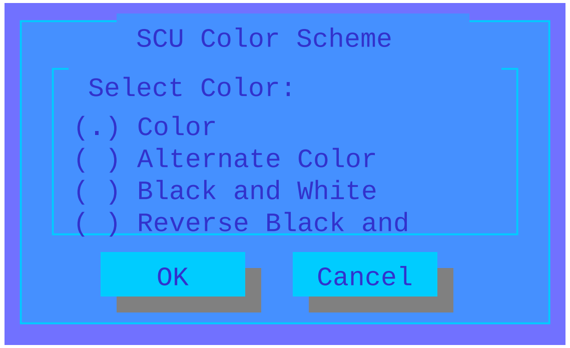
The procedure to set up the user password is the same as "Set Admin Password".

❖ **NOTE:**

1. You can not set up the user password unless the administrator password has been set up.
2. If both the administrator and user passwords are set up, only one password is required to boot the system
3. To modify the SCU settings, you have to enter the administrator password. The user password only allows you to browse the settings.
4. If the "Resume System" item is checked, the password is required only when the system is restored from "Suspend-to-disk" status.

@ **SCU Color Scheme**

The "Splach boot Logo" item select color set for your viewing. When this item is selected, the submenu will display as shown below:



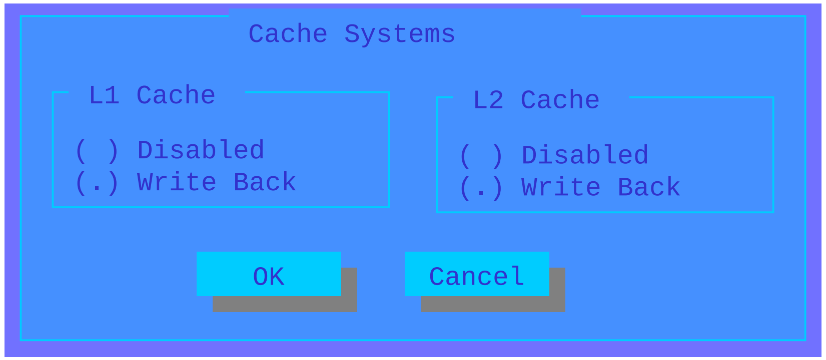
The default setting is "Color".

1.5.3.5 Memory Menu

Memory

Cache Systems >

@ **Cache System**



The default settings of the "L1 Cache" and "L2 Cache" are "Write Back".

1.5.3.6 Disk Menu

Disks

```
 √ Internal HDC
 √ IDE Setting          >
   Virus Alert          >
```

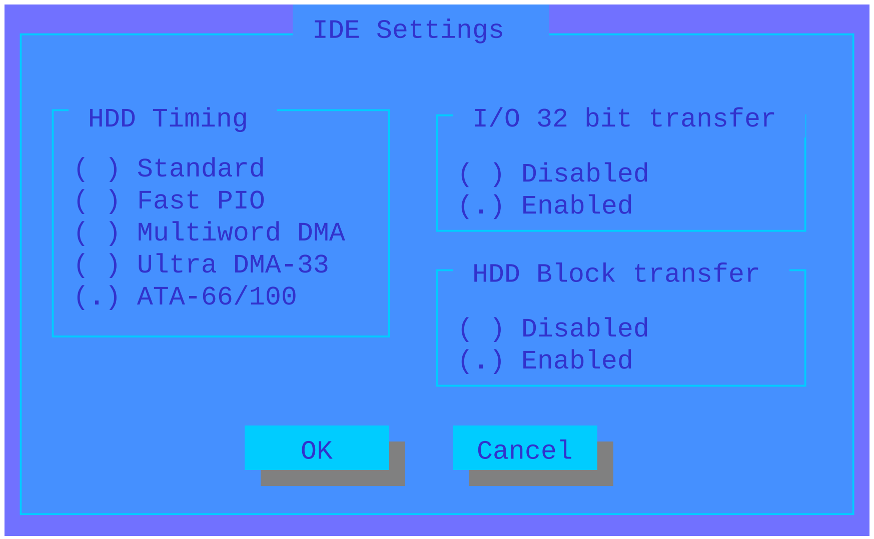
@ **Internal HDC**

The "Internal HDC" item sets if an internal hard drive is present.
When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates Disabled

The default setting is Enabled

@ **IDE Setting**

The "IDE Settings" item sets the type of the hard disk drive in your system. When this item is selected, the submenu will display as show below:



The “HDD Timing” item sets the data transmit mode of the hard drive. The default setting is Ultra DMA-33
The “I/O 32 bit transfer” item, if enabled, allows you to have better data transfer rate. This effect is more noticeable under DOS system. The default setting is Enabled

The “HDD Block transfer” item, if enabled, allows you to use hard disk with large capacity. The default setting is Enabled

@ **Virus Alert**

The “Virus Alert” item, when enabled, gives warning messages if the hard disk boot sector (partition table) has been changed

When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates disabled

The default setting is Disabled.

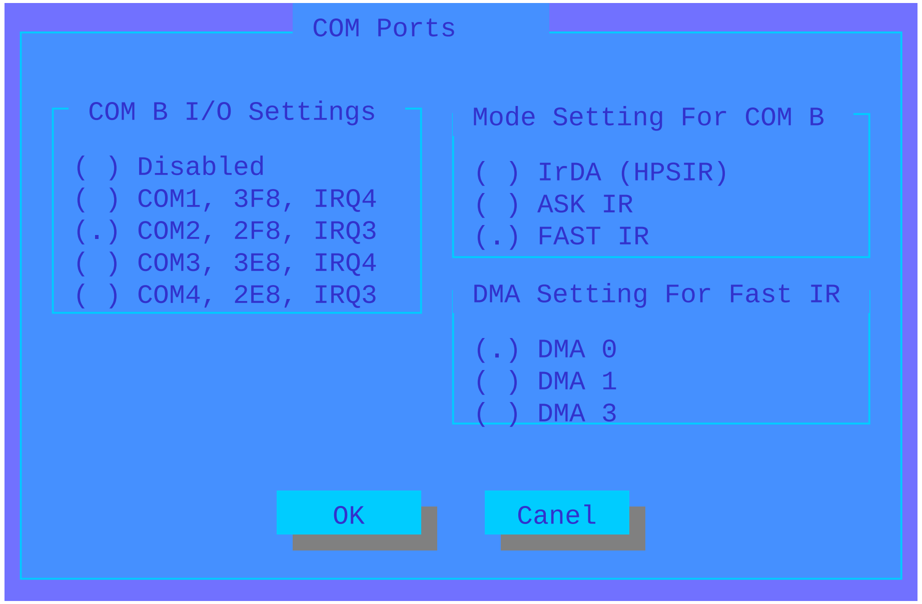
1.5.3.7 Components

Components

```
   COM Ports        >
   LPT Port
 √ PS/2 Mouse Port
   Legacy Usb       >
 √ Keyboard Numlock
   Keyboard Repeat  >
```

@ **COM Ports**

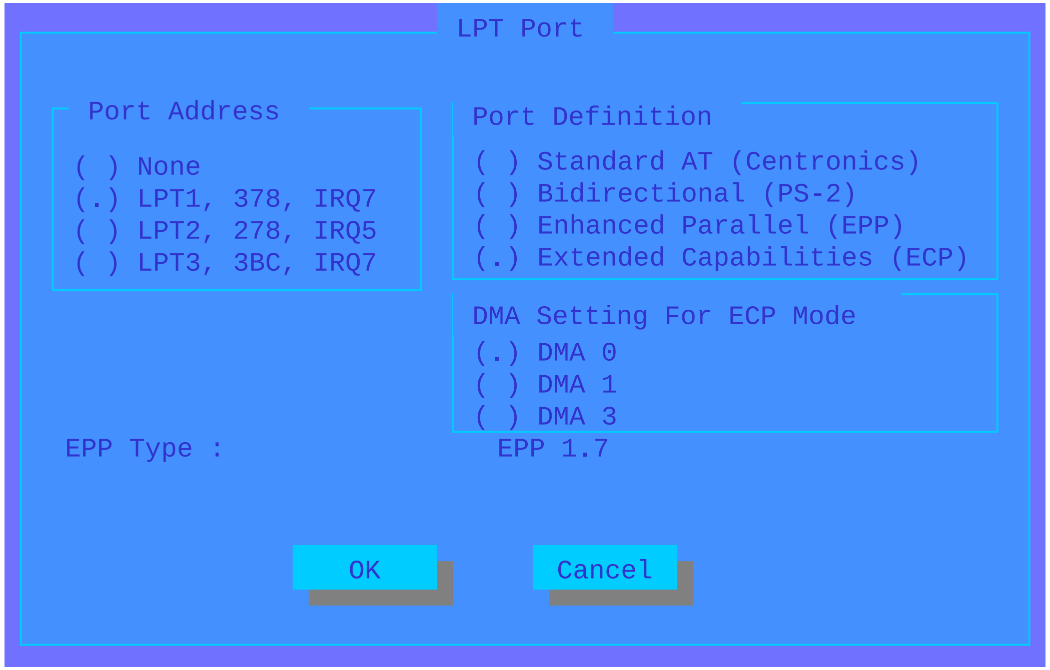
The “COM Ports” item sets the settings of COM Port A and B. When this item is selected, the submenu will display as shown below:



COM B is assigned to IR function. You can further select the IR mode in "Mode Setting for COM B" item and DMA channel in"DMA Setting For Fast IR" when you select "Fast IR" in the mode setting.

@ **LPT Ports**

The "LPT Port" item sets the settings of LPT port. When this item is selected, the submenu will display as shown below:



Your system supports EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port) standards which turn the standard parallel port into a high speed bi-directional peripheral port. If you select ECP item, you can further choose which DMA channel to use.

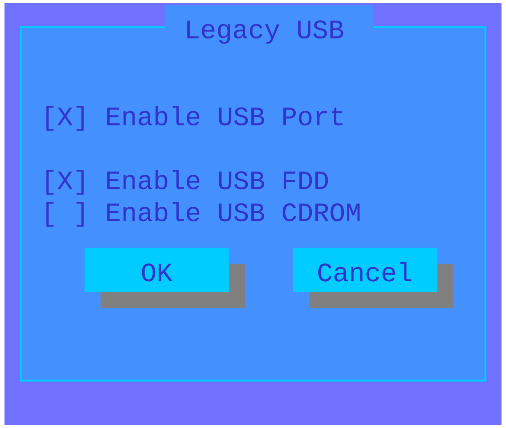
@ **PS/2 Ports**

The "PS/2 Mouse Port" item enables or disables the PS/2 mouse port

When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates Disabled. The default setting is enabled.

@ **Legacy USB**

The "Legacy USB" item sets the settings of legacy USB port which enables or disables the USB keyboard, USB mouse, USB floppy and USB CD-ROM in DOS and SCU. When this item is selected, the submenu will display as shown below:



The "Enable USB Port" item enables or disables USB keyboard and USB mouse. The default setting is enabled

The "Enable USB FDD" item enables or disables USB FDD. The default setting is enabled.

The "Enable USB FDD" item enables or disables boot from USB CDROM. The default setting is disabled

@ **Keyboard Numlock**

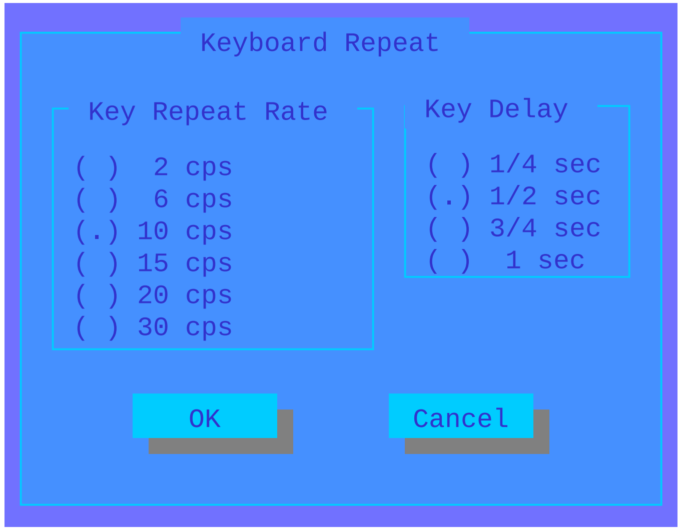
Keyboard Numlock" item sets if the numeric keypad will function

When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates Disabled. The default setting is Enabled.

❖ **Note:** If you disable this option, you can only activate the numeric keypad by holding down the [Fn] key first, even when the Num Lock indicator is on. However, an externally-connected keyboard is not affected by this feature.

@ **Keyboard Repeat**

The "Keyboard Repeat" item sets the repeat rate and delay time of key strokes. When this item is selected, the submenu will display as shown below:



The "Key Repeat Rate" sets the repeat rate when you hold down a key, while the "Key Delay" item sets the delaying time between key repeats

1.5.3.8 Power Menu

The Power pull-down menu, as shown below, contains the Power Management settings which help save power

Power

√	Enable Power Saving	
	Low Power Saving	
	Medium Power Saving	
	High Power Saving	
√	Customize	>
	Suspend Controls	>
	Resume Timer	>

@ **Enable Power Saving**

The “Enable Power Saving” item is the master control for the Power Management features. If this item is disabled, all Power menu items except “Suspend Controls” will be automatically disabled.

When this item is selected, no submenu will display. A check mark (√) indicates Enabled; an underline (_) indicates Disabled. The default setting is enabled

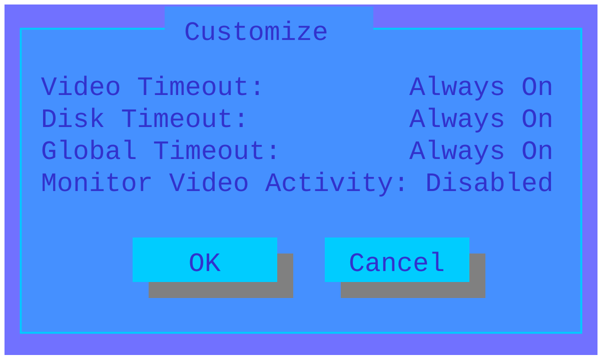
@ **Low Power Saving / Medium Power Saving / High Power Saving / Customize**

four items are mutually-exclusive options. You can select one of them. A check mark (√) indicates Enabled; an underline (_) indicates is enabled an underline (_) indicates Disabled

Descriptions of the four options are:

Options	**Descriptions**
Max Performance	Select this option for the pre-defined settings which allow maximum performance but shortest battery life.
Balanced Power Saving	Select this option for the pre-defined settings which allow moderate performance and moderate battery life.
Max Power Saving	Select this option for the pre-defined settings which allow longest battery life but minimum performance.
Customize	Select this option for setting up your own preferences. When this option is selected, the submenu will display as shown below that allows you to set up Power Saving features. (See the next subsection for information.)

❖ **Note:** Under Windows98/Windows Me/Windows2000, have built-in ACPI configurations which will override these settings When the "Customize" item is selected, the submenu will display as shown below:



Video Timeout :

The "Video Timeout" item sets the time-out period for the monitor to power down if it is not in use during the set period. The monitor will power up again when any key is pressed.

The available options are 30 Sec, 2 Min, 5 Min, 10 Min, 15 Min, 30 Min and Always On.

Disk Timeout:

The "Disk Timeout" item sets the time-out period for the hard disk to power down if it is not in use during the set period. The hard disk will power up again when next accessed.

The available options are 30 Sec, 1 Min, 1.5 Min, 2 Min, and Always On.

Global Timeout:

The "Global Timeout" item sets the time-out period for initiating Standby mode. Whenever the system. begins idling, the Power Saving starts the time-out for the Standby mode. If the system has been idled for the specified time-out period, system will enter Standby mode.

If Standby mode is in effect, several system subsystems go into standby or off mode so that system power will be reduced. The system will wake up from Standby mode when system activity is detected.

The available options are 1 Min, 2 Min, 4 Min, 6 Min, 8 Min, 12 Min, 16 Min, and Always On.

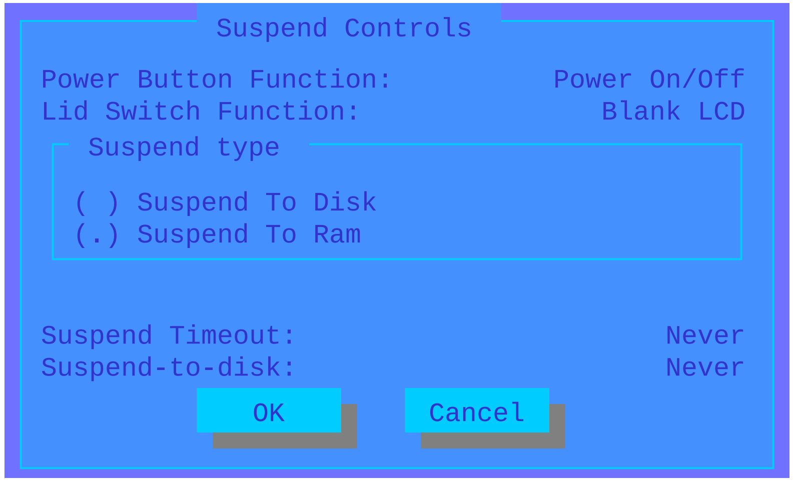
Monitor Video Activity

The "Monitor Video Activity" item sets if the video activity will be monitored. If enabled, any activity on the screen (such as showing a movie title) will prevent the monitor from powering down.

The available options are Enabled and Disabled.

@ Suspend Controls

The “Suspend Controls” item lets you micromanage several suspend features. When this item is selected, the submenu will display as shown below:



Power Button Function :

This item sets the function of the power button. The available options are Power On/Off and Suspend/ Resume.

❖ **Note:** When this item is set to “Suspend/Resume”, you can turn off the power by pressing the button for 4 seconds.

Lid Switch Function :

This item sets the sequential event when the top cover is closed while power is on. The available options are Blank LCD, Suspend and CRT/TV Display.

Suspend Type:

This item sets the suspend mode the system will enter. The available options are Suspend To Disk, Suspend To RAM.

When Suspend-to-RAM mode is initiated, several subsystems will enter standby or power-off mode to conserve power**.** The system will wake up from Suspend-to-RAM mode when a key is pressed. " Resume Timer", if enabled, can also wake up the system from Suspend-to-RAM mode.
When Suspend-to-Disk mode is initiated, the system preserves all the running application programs as a file in a "suspend-to-disk partition" on the hard disk and then turns off automatically.

Suspend Timeout :

The "Suspend Timeout" item sets the time-out period for initiating suspend mode. This item works in conjunction with previous "Global Timeout" item. When the system enters standby mode, the Power Saving starts the time-out for the Suspend mode. If the system has been in standby mode for the specified time-out period, system will enter Suspend mode.

The Suspend mode is determined by the "Suspend Type" item in the "Suspend Controls" submenu. It can be Suspend-to-RAM, Suspend-to-Disk.

The available options are 1 Min, 5 Min, 10 Min, 20 Min, 20 Min, 30 Min, and Never.

Suspend-to-disk:

The "Suspend-to-disk" item sets the time-out period for initiating suspend-to-disk mode. This item works in conjunction with previous "Suspend Timeout" item. When the system enters suspend-to-ram mode, the Power Saving starts the time-out for the Suspend-to-disk mode. If the system has been in suspend-to-ram mode for the specified time-out period, system will enter suspend-to-disk mode.

The available options are 1 Min, 5 Min, 10 Min, 20 Min, 30 Min, and Never.

@ **Resume Timer**

The Resume Timer" item sets the date and time the system will resume from suspend mode. When this item is selected, the submenu will display as shown below :

```
              Resume Timer

Alarm Resume :    Disable
    Resume Month        8
    Resume Day          8
    Resume Hour        12
    Resume Minute       0

   OK           Cancel
```

The default setting is Disabled

1.5.3.9 Exit Menu

The Exit pull-down menu, as shown below, displays ways of exiting SCU. After finished with your settings, you must save and exit SCU so that the settings can take effect

Exit

```
   Save and Exit    >
   Exit (No Save)   >
   Default Settings >
   Restore Settings >
   Version Info     >
```

Descriptions of the Exit choices are:

Choices	**Descriptions**
Save and Reboot	Save changes and reboot the system.
Exit (No Save)	Exit without saving the changes you have made.
Default Settings	Load factory default values for all the items.
Restore Settings	Restore previous values for all the items.
Version Info	Show BIOS version information

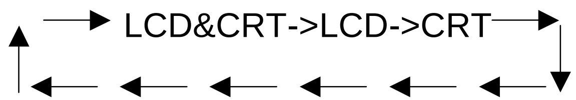
1.5.4 Function Hotkeys

Fn + F5	Toggle display output. The display switch sequence, please refer to chapter 6
Fn + F6	Brightness Down (16 levels)
Fn + F7	Brightness Up (16 levels)
Fn + F10	Enable/Disable battery warning beep
Fn + F11	Panel on/off
Fn + F12	Suspend to RAM or disk

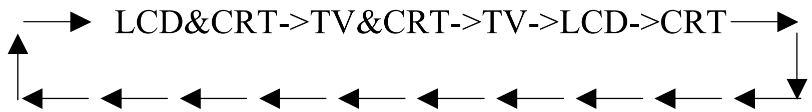
1.5.5 Display Out

When you boot the system with CRT, display output is LCD&CRT mode.

When boot with CRT, the display switch sequence by hotkey FnF5 is as following:



When boot with CRT and TV, the display switch sequence by hotkey FnF5 is as following:



1.5.6 LID

@ ***In Non-ACPI Operating System:***

LID switch function is dependent on the setting in BIOS setup menu.

"Blank LCD" - LCD will be blank when LID is closed.

Before LID is closed	***LID is closed***	***LID is opened***
LCD is active	LCD is blank	LCD is active
LCD is blank	LCD is blank	LCD is blank

"Suspend" -system will enter suspend mode when LID is closed.

Before LID is closed	***LID is closed***	***LID is opened***
System is On	System enters Suspend	System still in Suspend
System in Suspend	System still in Suspend	System still in Suspend

"CRT/TV Display" -display will be switched to CRT/TV when LID is closed.

When the LID is closed, the LCD will be inactive and external display device will be active.

When the LID is opened, the display devices status (active/inactive) will be restored to the state before the LID is closed.

Some special conditions are list below.

Before LID is closed	***LID is closed***	***LID is opened***
LCD (active) CRT (present, inactive) TV(present, inactive)	LCD (inactive) CRT (active) TV(inactive)	LCD (active) CRT (inactive) TV(inactive)
LCD (inactive) CRT/TV is present	LCD (inactive) CRT/TV is plugged out	LCD (active) CRT/TV is not present

@ ***In ACPI Operating System:***

The LID switch function is dependent on the setting of the Power Management in the operating system.

1.5.7 VGA Resolution of Windows 98/Me Driver (Need Modifying via VGA Driver)

LCD(LCD&CRT)

Resolution	Color
640*480	256, 16bit, 32bit
800*600	256, 16bit, 32bit
1024*768	256, 16bit, 32bit

CRT(TV)

Resolution	Color
640*480	256, 16bit, 32bit
800*600	256, 16bit, 32bit
1024*768	256, 16bit, 32bit
1280*1024	256, 16bit
1600*1200	256, 16bit

TV(TV+CRT)

Resolution	Color
640*480	256, 16bit, 32bit
800*600	256, 16bit, 32bit

1.5.8 LED Indicators

System has nine status LED indicators to display system activity which include below LCD panel unit and above keyboard:

1.5.8.1 Three LED indicators below LCD panel unit:

From left to right that indicate AC POWER, BATTERY POWER and BATTERY STATUS

® **AC POWER:** This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.

® **BATTERY POWER:**This LED lights green when the notebook is being powered by batteries, and flashes (on 1 second, off 1 second) when Suspend to DRAM is active using battery power. The LED is off when the notebook is off or powered by AC, or when Suspend to Disk.

® **BATTERY STATUS:**During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.

1.5.8.2 Five LED indicators in front of palm rest:

From left to right that indicates CD-ROM/MO, HARD DISK DRIVE, , NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.5.8.3 Mail/Blue-Tooth LED indicators in front of palm rest:

The left side green LED flashing means new mail coming. Otherwise the LED is always OFF. The right side red LED ON means Blue-Tooth module turn ON.

1.5.9 Power Management

1.5.9.1 Features

® APM 1.2/1.1/1.0 compliant
® Battery warning beep
® Battery low suspend to RAM/disk
® Cover switch close to panel off, standby, or suspend
® Hot-key suspend
® Hot-key panel on/off
® Auto clock throttling to prevent overheating
® ACPI 1.0 compliant
® User programmable standby/suspend timers and sustained events when OS doesn't support APM/ACPI

1.5.9.2 Device power state

Note: Each device power states are described in the chapter titled Components & Drives. Please refer to those paragraphs. BIOS will not automatically manage devices' power states if ACPI engaged or APM engaged but disabled.

1.5.9.3 System power state

Definitions when ACPI engaged

Global States:

G0 – Global system is working

G1 – Global system is sleeping

G3 – Global system is mechanical-off

Suspend States:

S1 – CPU stop, no system context lost

S2 – CPU stop, no system context lost except CPU & cache's context is lost

S3 – CPU stop, the whole system context lost except system memory content is maintained

S4 – CPU stop, all system context saved to nonvolatile media before lost.

S5 – Soft Off

CPU States:

C0 – CPU is working

C1 – CPU is in Auto Halt Mode

C2 – CPU is in Quick Start Mode, the system will maintain the cache coherency

C3 – CPU is in Deep Sleep Mode, the system must disable any event which could make the cache lost coherency. This model is not support C3 mode.

1.5.9.4 Definitions when APM engaged

System States:

Full On	-Full running state, the system is in optimized performance
Idle	-Clock throttling state, CPU is running between C0 & C2 states
Standby	-Same as S1/S2 above
Suspend	-Same as S3 above (Including save-to-ram and power-on-suspend)
Save to Disk	-Same as S4 above

❖ **Note:** When Save to Disk partition is not made on disk, BIOS will choose Save to RAM instead of Save to Disk

Enter Condition:

Idle	-Entered when CPU Idle Function is called
Standby	-Entered when SetPowerState(Standby) Function is called
Suspend	-Entered when SetPowerState(Suspend) is called, and user select STR in SCU
Save to Disk	-Entered when SetPowerState(Suspend) is called, and user select STD in SCU

Resume Event :

Idle	-Resume when CPU Busy Function is called
Standby	-Resume only when keyboard device have activities, when ring come in on internal modem or PCMCIA card. The reason for not selecting track-pad as resume event is that, it's too sensitive sometimes
Suspend	-Entered when SetPowerState(Suspend) is called, and user select STR in SCU
Save to Disk	-Entered when SetPowerState(Suspend) is called, and user select STD in SCU

***Event Notifications*:**

Standby -When all the devices have no system activities for a specific time period, BIOS will inform a standby event once OS calls GetPMEvent Function.

Suspend -When all the devices have no system activities for a specific time period, BIOS will inform a suspend event once OS calls GetPMEvent Function.

Activities -System activities is defined in SCU one by one. SCU also includes two columns for the time periods for Standby and Suspend. In addition, Keyboard activity is always one of the system activities. Whenever any system activities detected, timers for Standby and Suspend are reloaded into the value specified. By the way, RTC could also programmable to wake up the system from Standby and Suspend states.

Exception -Note, when APM is disabled, BIOS should disable all timers and not to automatically power manage devices. Furthermore, the APM BIOS will neither response to CPU Idle Function, nor recognize the time periods set for Standby and Suspend in SCU.

1.5.9.5 Definitions when no APM or ACPI engaged

System States:

Full On -Full running state, the system is in optimized performance

Idle -No Idle mode support in this situation .

Standby -Same as S1/S2 above

Suspend -Same as S3 above (Including save-to-ram and power-on-suspend)

Save to Disk -Same as S4 above

❖ **Note:** When Save to Disk partition isn't made on disk, BIOS will choose Save to RAM instead of Save to Disk

Resume Event:

Standby -Resume when keyboard/trackpad/PS2 devices have activities, when ring come in on internal modem or PCMCIA card, or when COM has activities if user select to resume from COM port

Suspend -Same as resume events for Standby state

Save to Disk -Resume when User push power button

Enter conditions:

-The timers for Standby and Suspend mode when APM engaged are also applied to this situation that no APM or ACPI engaged.

Special Events:

-Cover switch, or called lid could trigger an event to LCD panel off, Standby(S1/S2), or Suspend(S3/S4). The exact state triggered is selected in SCU

-Power button is also a resume event for all power saving mode except the Idle state

-When battery capacity is low under 10% while AC is not plug-in, system will begin to alert via PC speaker. User could also press Fn+F10 to disable/enable the warning beep. Once the battery capacity is critically under 3%, system BIOS will try to force the whole system into the STD state.

1.5.9.6 Save to disk partition utility

0VMAKFIL.EXE S support partition only

Usage: 0VMAKEFILE.EXE -P<partition size>

< Partition size>= total of system RAM size + total of video RAM size

1.5.9.7 ACPI

@ **Custom Software SMI Command for ACPI(Modifying if Need)**

(1) 0x81 : Notify BIOS that the system is going to enter S3

(2) 0x82 : Notify BIOS that the system wake up from S3

(3) 0x83 : Get AC Status

(4) 0x84 : Get Battery General Status (_STA)

(5) 0x85 : Get Battery Information (_BIF)

(6) 0x86 : Get Battery Present Status (_BST)

(7) 0x87 : Get Battery Trip Point (_BTP)

@ **CMOS mapping for ACPI battery control method to use (Modifying if Need)**

Index	Description	Comment
0x40	AC Status	Bit0: 0 – AC present 1 – AC not present
0x41	Battery Info 1	Bit0: Bit1: 0 – NiMH 1 – LiON
0x42	Battery Info 2	Bit0: 0 – Battery not present 1 – Battery present Bit1: Bit2: 0 – no force charge 1 – force charge Bit3:
0x43	Battery Info 3	Bit0: 0 – no trickle charge 1 – trickle charge
0x44~0x45	Last Full Charge Capacity	
0x46~0x47	Remaining Capacity	
0x48~0x49	Design Capacity	
0x4A~0x4B	Design Voltage	
0x4C	SOC1	
0x4D	Current Voltage	
0x4E	Battery Trip Point	

1.5.10 Post Massage

Reference to 7.2

1.5.11 GPIO settings

1.5.11.1 South Bridge

@ **GPIO Signal**

I/O Address GPIO Register I/O Address Map

GPIO #	Multi. Func./Note	Type	Signal Name / Description	Signal Select Register
0	REQ[A]#	I		
1	REQ[B]#/REQ[5]#	I		
2	Not Implement	N/A		
3	PIRQ[F]#	I		
4	PIRQ[G]#	I		
5	Not Implement	N/A		
6		I		
7		I		
8		I	SCI#	
9	Not Implement	N/A		
10	Not Implement	N/A		
11	SMBALERT#	I		
12		I	EXTSMI#	
13		I		
14	Not Implement	N/A		
15	Not Implement	N/A		
16	GNT[A]#	O		
17	GNT[B]#/GNT[5]#	O		
18		O		
19		O	ENABKL_MSK#	
20		O	CDROM_PWRON#	
21		O	HDD_PWRON#	

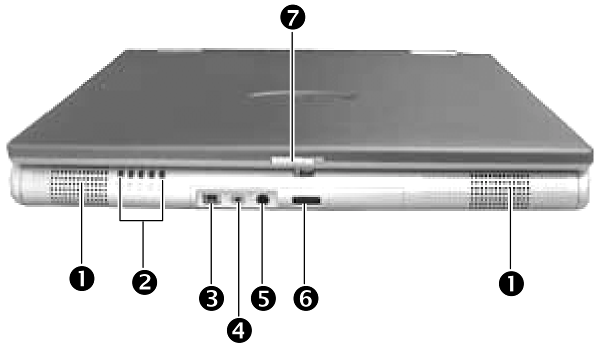
22		O	DRAMENA	
23		O		
24		I/O	1394WR#	GPIOBASE+04 bit24 = 0
25		I/O	PCIRST_MSK#	GPIOBASE+04 bit25 = 0
26	Not Implement	N/A		
27		I/O	GATE1394#	GPIOBASE+04 bit27 = 0
28		I/O	SPK_OFF	GPIOBASE+04 bit28 = 0
29	Not Implement	N/A		
30	Not Implement	N/A		
31	Not Implement	N/A		

2. System Assembly & Disassembly

2.1 System View

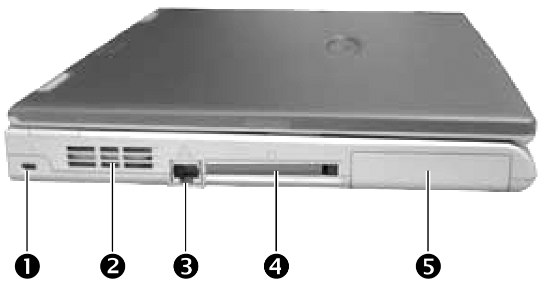
2.1.1 Front View

❶ Stereo Speaker Set
❷ Device Indicators
❸ Mini IEEE1394 Connector
❹ Audio Input Connector
❺ Line Out Phone Jack
❻ Volume Control
❼ Top Cover Latch



2.1.2 Left-Side View

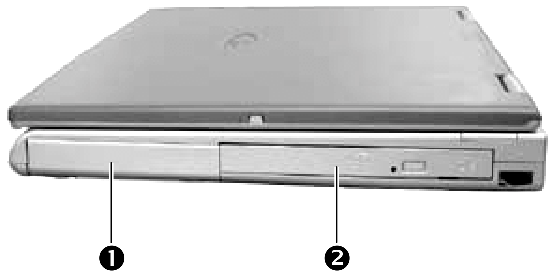
❶ Kensington Lock
❷ Ventilation Openings
❸ RJ-45 Connector
❹ PC Card Slot
❺ Hard Disk Drive



2.1.3 Right-Side View

❶ Battery Pack

❷ CD-ROM/DVD-ROM Drive



2.1.4 Rear View

❶ Power Connector

❷ S-Video Output Connector

❸ USB Ports

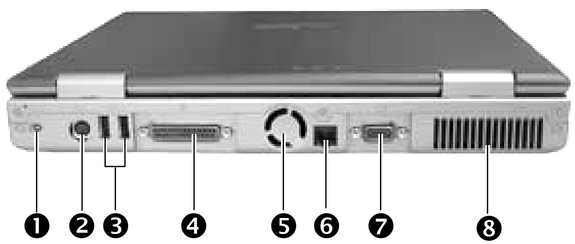
❹ Parallel Port

❺ D/D Fan

❻ RJ-11 Connector

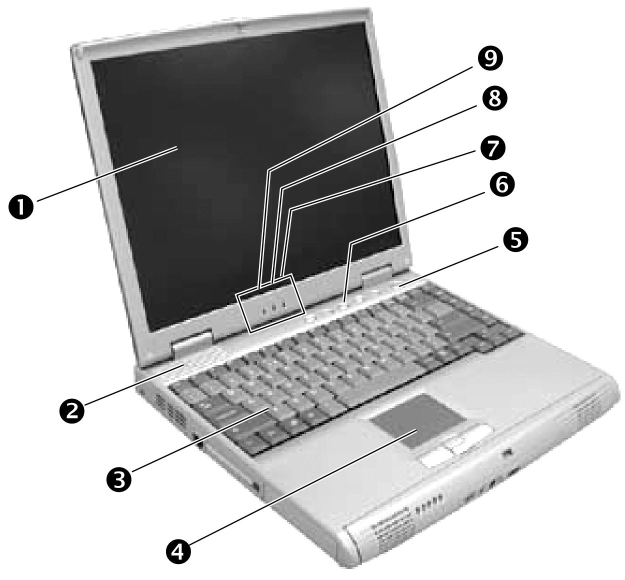
❼ VGA Port

❽ Ventilation Openings



2.1.5 Top-Open View

❶ LCD Screen
❷ Microphone
❸ Keyboard
❹ Touch pad
❺ Power Button
❻ Easy Start Buttons
❼ Battery Charge Indicator
❽ Battery Power Indicator
❾ AC Power Indicator



2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

- **NOTEBOOK**
  - **Modular Components**
    - **2.2.1 Battery Pack**
    - **2.2.2 Keyboard**
    - **2.2.3 CPU**
    - **2.2.4 HDD Module**
    - **2.2.5 CD/DVD-ROM Drive**
    - **2.2.6 SO-DIMM**
  - **LCD Assembly Components**
    - **2.2.7 LCD Assembly**
    - **2.2.8 LCD Panel**
    - **2.2.9 Inverter Board**
  - **Base Unit Components**
    - **2.2.10 System Board**
    - **2.2.11 Touch pad**
    - **2.2.12 Modem Card**

2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the release lever to the "unlock" (🔓) position (❶), then slide and hold the release lever outwards and pull the battery pack out of the compartment (❷). (Figure 2-1)

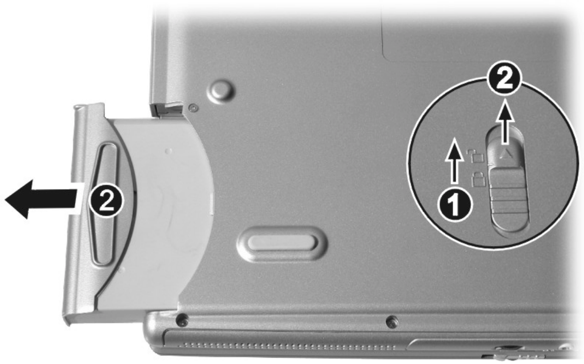


Figure 2-1 Remove the battery pack

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" (🔒) position.

2.2.2 Keyboard

Disassembly

1. Insert a small rod, such as a straightened paper clip, into the eject hole near the power connector of the notebook. (Figure 2-2)



Figure 2-2 Insert a rod easy to remove LED Panel

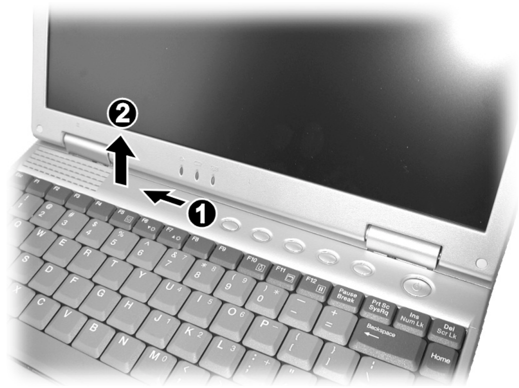


Figure 2-3 Remove LED Panel

2. Open the top cover. Push the rod firmly and slide the LED panel to the left (❶). Then lift the LED panel up from the left side (❷) (Figure 2-3)

3. Remove three screws fastening keyboard on the base unit cover. (Figure 2-4)
4. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-5)

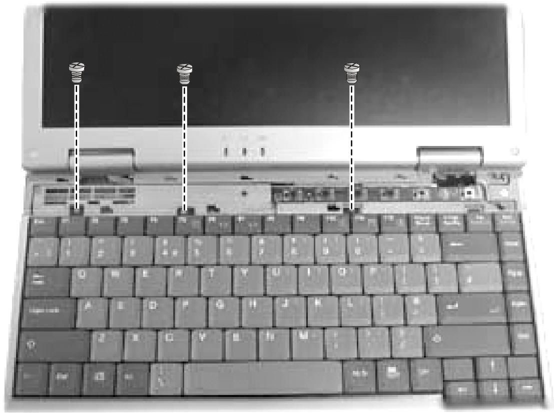


Figure 2-4 Remove three Screws

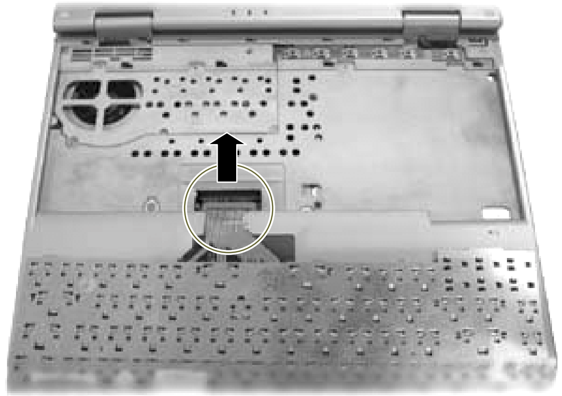


Figure 2-5 Remove keyboard

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the LED panel.

2.2.3 CPU

Disassembly

1. Remove the LED panel and keyboard to access the CPU compartment. (See section 2.2.2 Disassembly.)
2. Remove five screws locking the heatsink cover. (Figure 2-6)

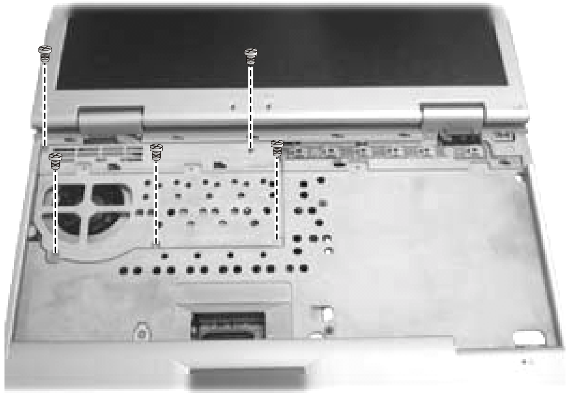


Figure 2-6 Remove the cover

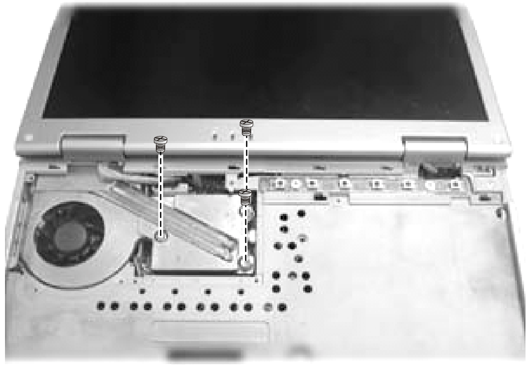


Figure 2-7 Remove the heatsink

3. Remove three screws locking the heatsink. (Figure 2-7)

4. Disconnect the fan's power cord from the system board, then lift up the heatsink. (Figure 2-8)

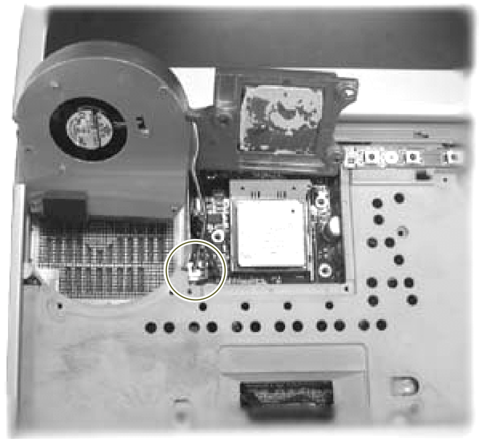


Figure 2-8 Remove the fan's power cord

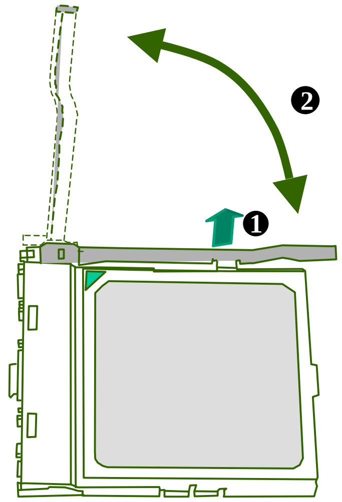


Figure 2-9 Remove the CPU

5. push the lever to the right. Then lift up the lever to the vertical position. Finally, remove the existing CPU.

Reassembly

1. Carefully, Align the arrowhead corner of the CPU with the beveled corner of the socket, then insert the CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left .
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with three screws.
3. Replace the keyboard .Then replace LED panel.

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw and slide the HDD module out of the compartment. (Figure 2-10)



Figure 2-10 Remove HDD Module

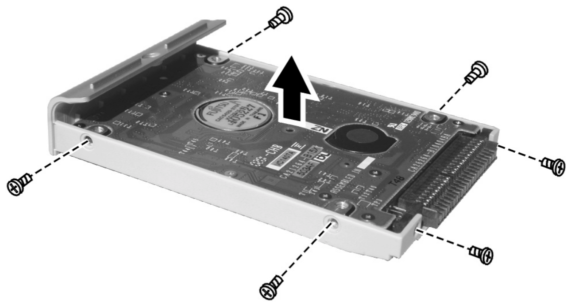


Figure 2-11 Disassemble the hard disk

3. Remove six screws to separate the hard disk drive from the metal shield. (Figure 2-11)

Reassembly

1. To install the hard disk drive, place it in the bracket and secure with six screws.
2. Slide the HDD module into the compartment and secure with one screw.

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Remove the LED panel and keyboard. (See section 2.2.2 Disassembly.)
2. Remove two screws locking the CD/DVD-ROM drive. (Figure 2-12)

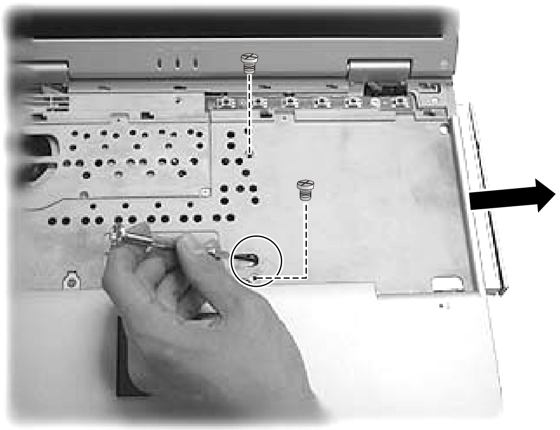


Figure 2-12 Push out the CD/DVD -ROM drive

3. Use the screwdriver to push the metal pad to the right and the CD/DVD-ROM drive will pop out. Hold the CD/DVD-ROM drive and slide it outwards carefully. (Figure 2-12)

Reassembly

1. Push the CD/DVD-ROM drive into the compartment.
2. Secure the CD/DVD-ROM drive with two screws.
3. Replace the keyboard and LED panel.

2.2.6 SO-DIMM

Disassembly

1. Carefully put the notebook upside down.
2. Remove four screws to access the SO-DIMM socket.
3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-13,14)



Figure 2-13 Remove the SO-DIMM Cover

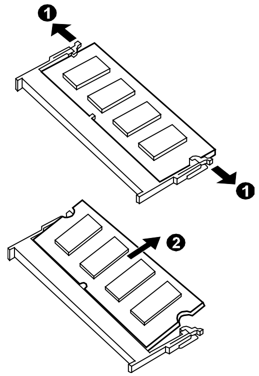


Figure 2-14 Remove the SO-DIMM

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace three screws to lock the SO-DIMM socket cover.

2.2.7 LCD Assembly

Disassembly

1. Open the top cover. Remove the LED panel, keyboard, and heat sink . (See section 2.2.2 and 2.2.Disassembly.)
2. Pull out the antenna from the CPU compartment.
3. Remove the two hinge covers. (Figure 2-15)

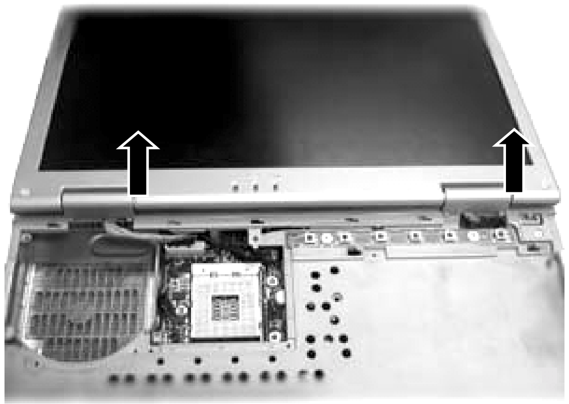


Figure 2-15 Remove the LCD hinge covers

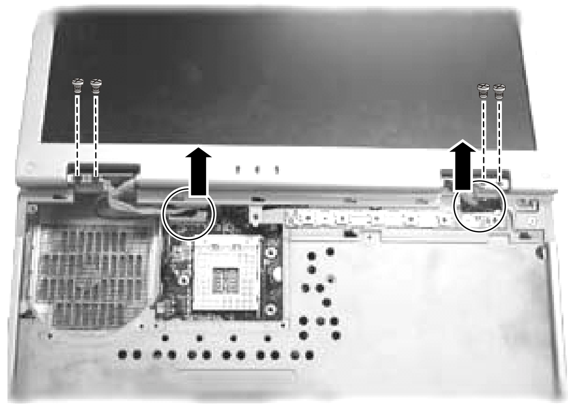


Figure 2-16 Remove cables and Screws to separate LCD

4. Disconnect the LCD cable from the system board, and remove four screws of the hinges. Now you can separate the LCD assembly from the base unit. (Figure 2-16)

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the antenna to the connector on the Mini PCI socket.
3. Reconnect the LCD cable to the system board.
4. Replace the heatsink, keyboard and LED panel.two hinge covers.
5. Replace two hinge covers.

2.2.8 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 2.2.7 Disassembly.)
2. Remove the four rubber pads and four screws on the corners of the panel. (Figure 2-17)



Figure 2-17 Remove LCD frame



Figure 2-18 Remove LCD panel

3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out.
   Repeat the process until the frame is completely separated from the housing.
4. Remove the two screws on two sides and two screws on the lower part of of the LCD panel, and disconnect the cable from the inverter board. (Figure 2-18)

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the four screws and four rubber pads.
3. Replace the LCD assembly. (See section 2.2.7 Reassembly.)

2.2.9 Inverter Board

Disassembly

1. Remove the LCD assembly. (see section 2.2.7 Disassembly.).
2. Detach the LCD Panel. (See section 2.2.8 Disassembly.)
3. To remove the inverter board on the bottom of the LCD assembly, disconnect the cable and remove one screw. (Figure 2-19)



Figure 2-19 Remove the Inverter Board

Reassembly

1. Fit the inverter board back into place and secure with one screw.
2. Reconnect the cable.
3. Replace the LCD frame. (See section 2.2.8 Reassembly.)
4. Replace the LCD assembly. (See section 2.2.7 Reassembly.)

2.2.10 System Board

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly.
   (See sections2.2.1; 2.2.2; 2.2.3; 2.2.4; 2.2.5; 2.2.7 Disassembly.)
2. Remove fourteen screws on the bottom of the notebook. (Figure 2-20)

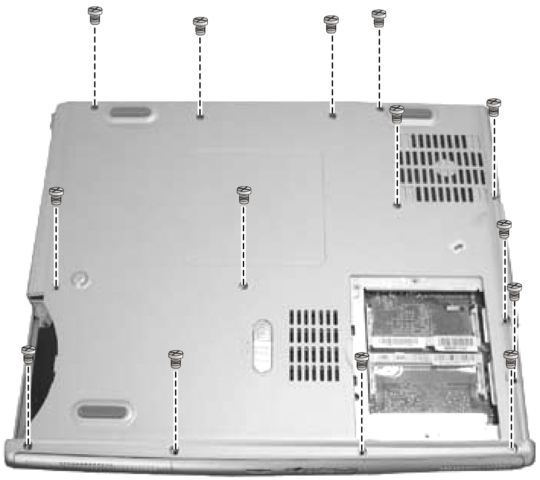


Figure 2-20 Remove the bottom

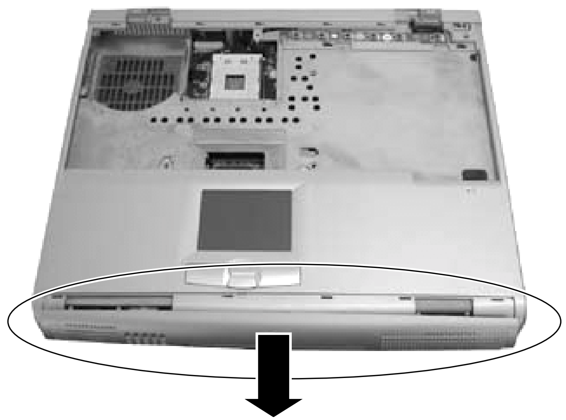


Figure 2-21 Remove the speaker assembly

3. Remove the speaker assembly from the notebook. (Figure 2-21)

4. Remove five screws on the rear side of the notebook, and remove three screws locking on the base unit cover. (Figure 2-22)

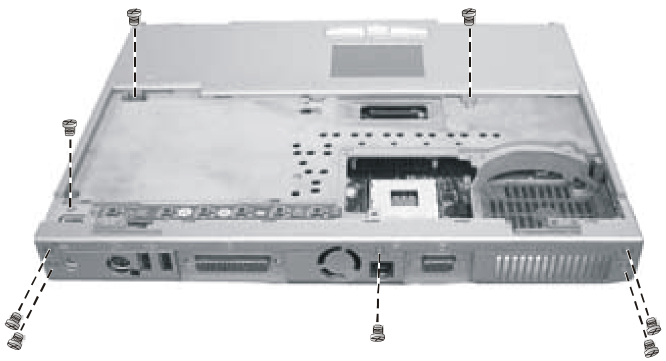


Figure 2-22 Remove the base unit cover

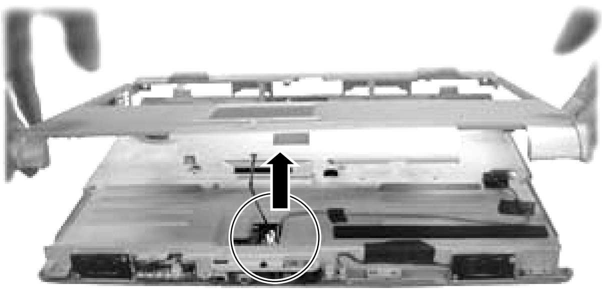


Figure 2-23 Lift up the base unit cover

5. Lift up the base unit cover and disconnect the touch pad cord. (Figure 2-23)

6. Remove two screws fastening the button board on base unit. and then disconnect two cables from the system board. (Figure 2-23)

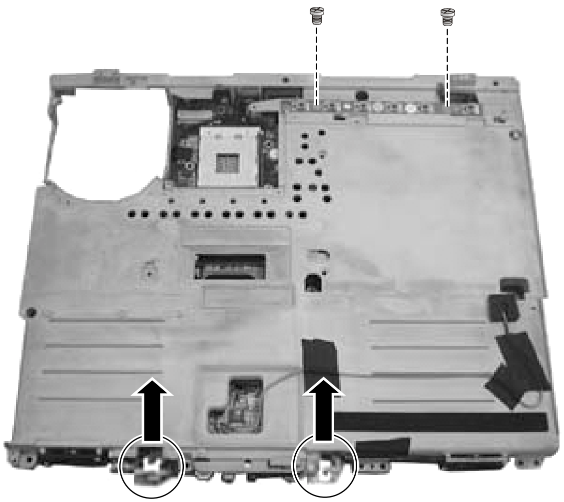


Figure 2-23 Remove the screws



Figure 2-24 Remove the base unit cover

7. Remove five screws from the system board,and lift up the base unit to access the system board. (Figure 2-24)

Reassembly

1. Replace five screws fastening the base unit
2. Reconnect two cables to the system board.
3. Replace the button board with two screws.
4. Reconnect the touch pad cable and replace the base unit cover.
5. Replace three screws fastening the base unit cover.
6. Replace five screws on the rear side of the notebook.

7. Replace the speaker assembly.
8. Replace fourteen screws on the bottom of the notebook.
9. Replace the battery pack, LED panel, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly.

2.2.11 Touch PAD

Disassembly

1. Remove the base unit cover. (See steps 1-6 in section 2.2.11 Disassembly.)
2. Remove the six screws to lift up the touch pad holder and touch pad panel. (Figure 2-25)

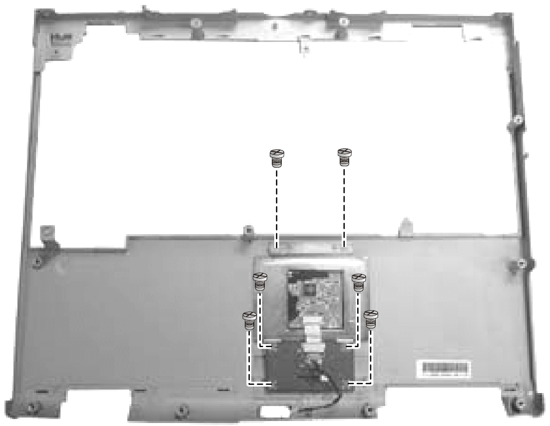


Figure 2-25 Remove the touch pad

Reassembly

1. Replace the touch pad holder and touch pad panel, and secure with six screws.
2. Assemble the notebook. (See section 2.2.11 Reassembly.)

2.2.12 Modem Card

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive, and LCD assembly.
   (See sections2.2.1; 2.2.2; 2.2.3; 2.2.4; 2.2.5; 2.2.7 Disassembly.)
2. Disassemble the notebook to access the system board. (See section 2.2.10 Disassembly.)
3. Remove the two screws fastening the modem card,and then disconnect the cable from system board. (Figure 2-26)

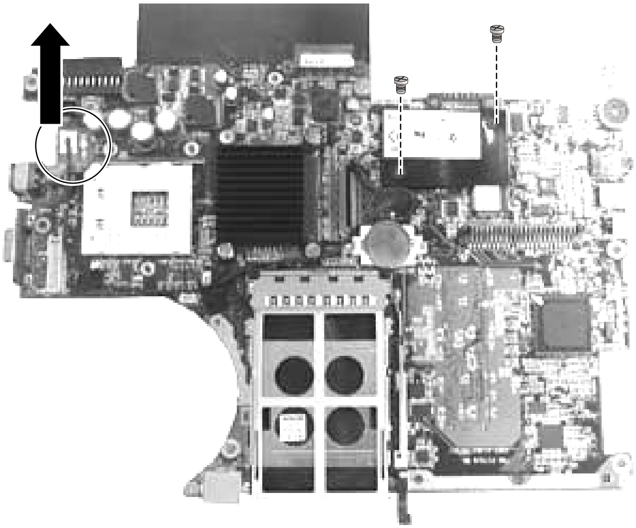


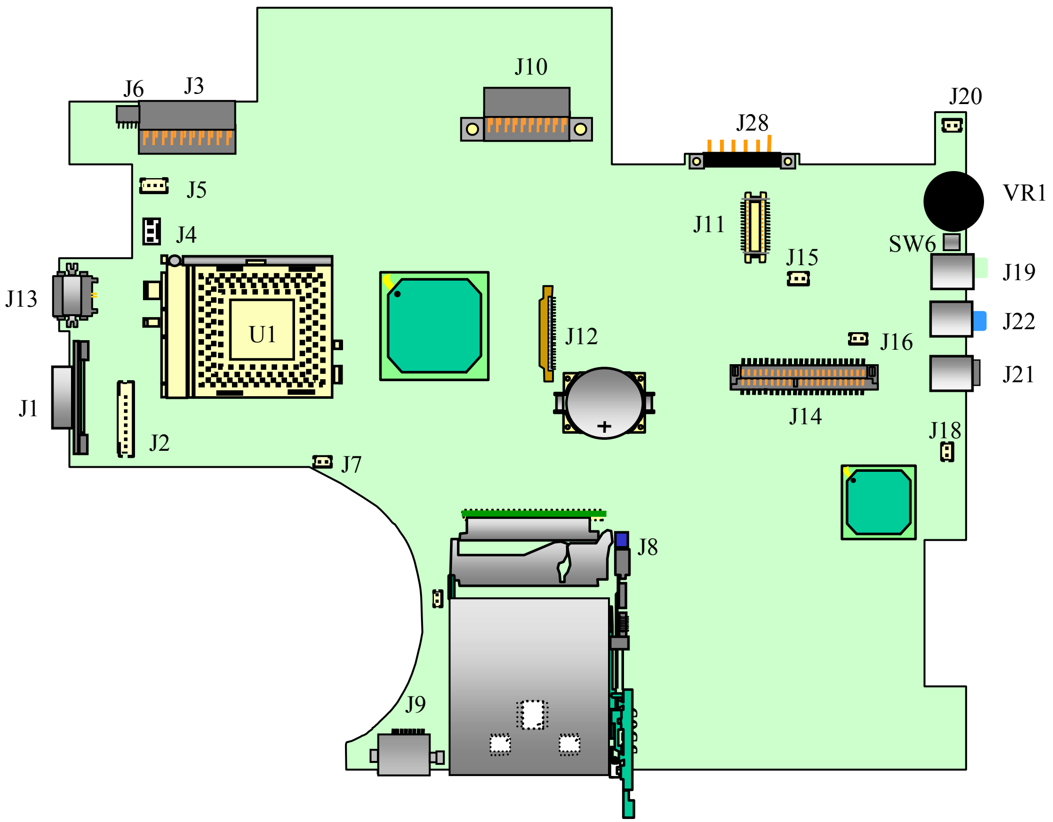
Figure 2-26 Remove the Modem card

Reassembly

1. Reconnect the cable to the modem card and secure the modem card with two screws.
2. Assemble the notebook. (See section 2.2.10 Reassembly.)

3. Definition & Location Connectors / Switches Setting

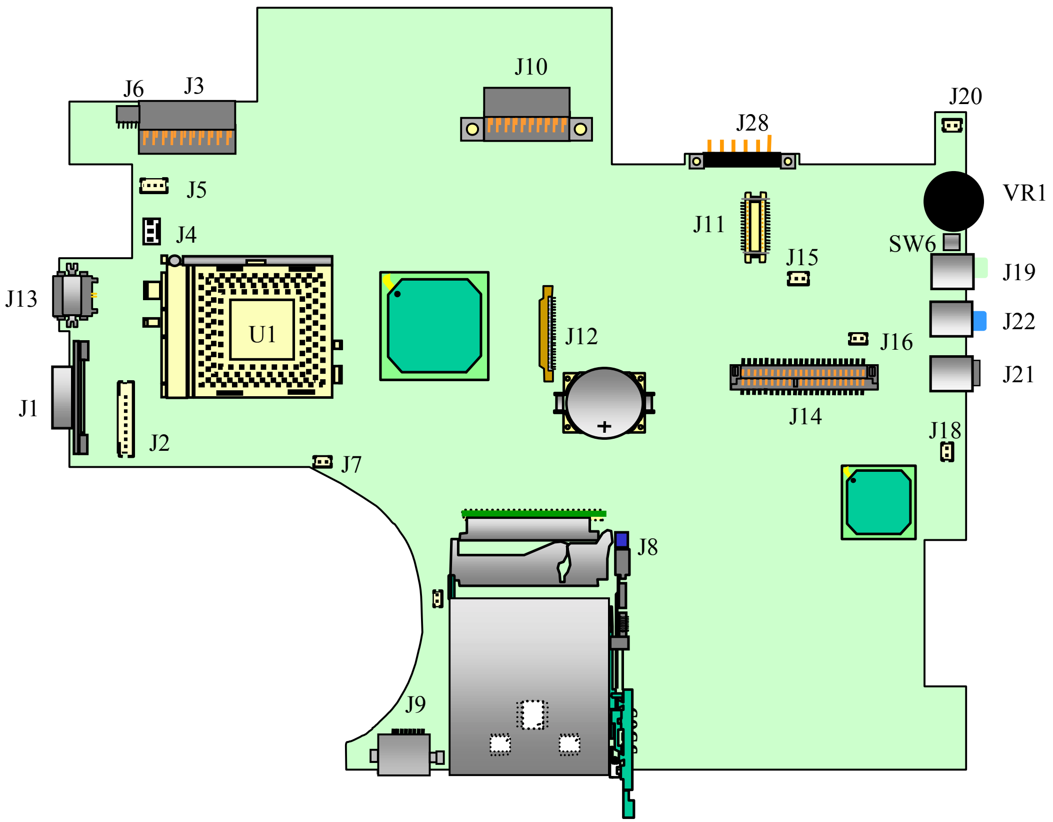
3.1 Main Board (Side A)



- J1:External VGA Connector
- J2:LCD Connector
- J3:D/D Board connector
- J4: Modem Daughter Board to RJ11Connector
- J5:Easy Start Button Connector
- J6:External USB(PIO,IR,TV OUT)Connector
- J7:CPU FAN Connector
- J8:Card Bus Socket
- J9:RJ45
- J10:Secondary EIDE Connector
- J11:Modem Daughter Board
- J12:Internal Keyboard Connector
- J13:RJ11

3. Definition & Location Connectors / Switches Setting

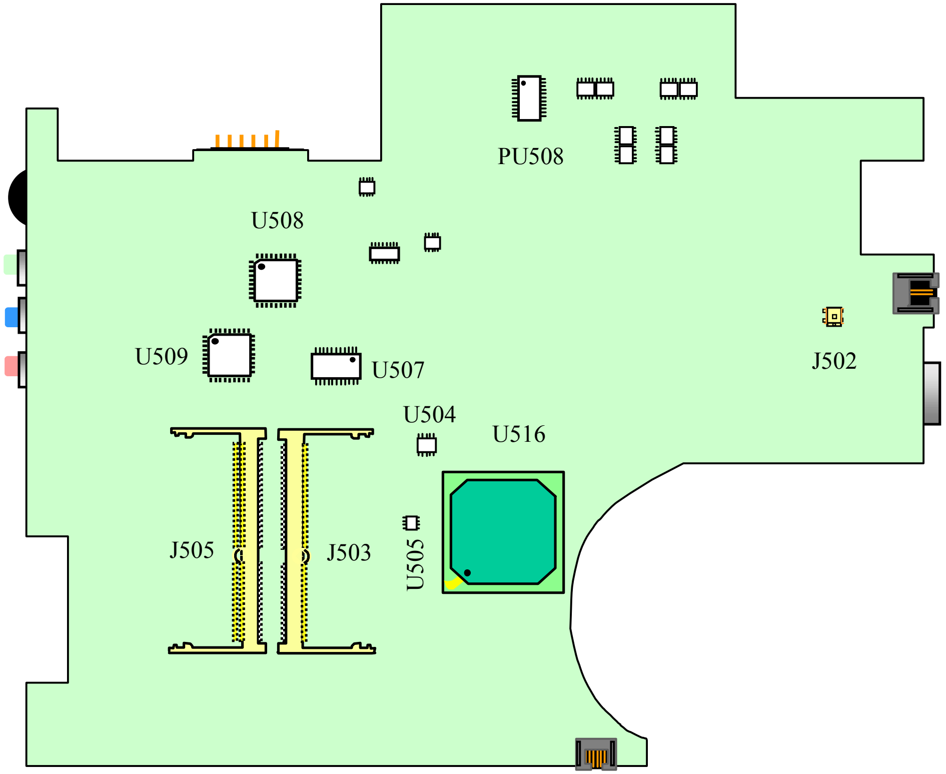
3.1 Main Board (Side A)



- J14:Primary EIDE Connector
- J15:Touch PAD Connector
- J16:Internal Microphone
- J18:Internal Speaker Connector(L channel)
- J19:Line Out Phone Jack
- J20:Internal Speaker Connector(R channel)
- J21:Mini IEEE1394 Connector
- J22:External Micro Phone Jack
- J28:Battery Connector
- VR1:Volume regulator
- SW6:Switch Cover

3. Definition & Location Connectors / Switches Setting

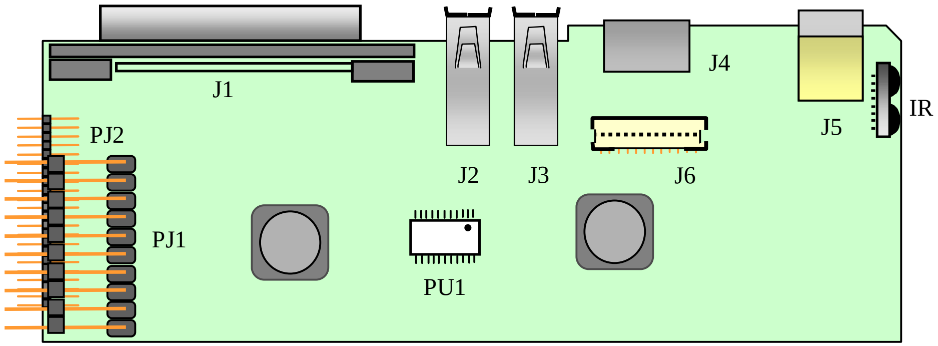
3.1 Main Board (Side B)



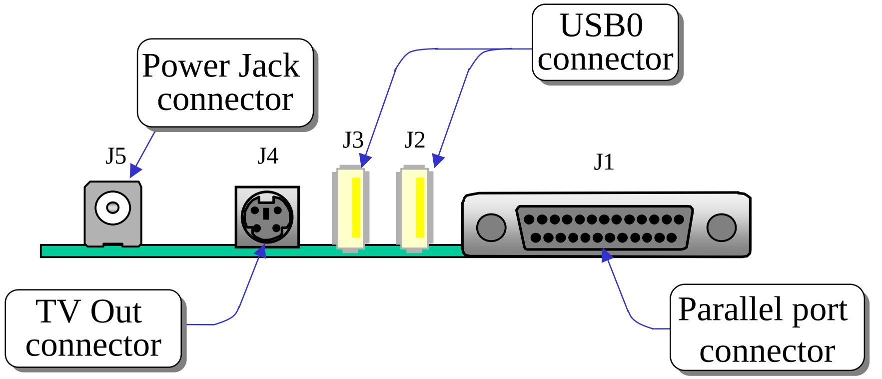
- J502:D/D FAN connector
- J503:DIMM1
- J505:DIMM2

3. Definition & Location Connectors / Switches Setting

3.2 D/D Board



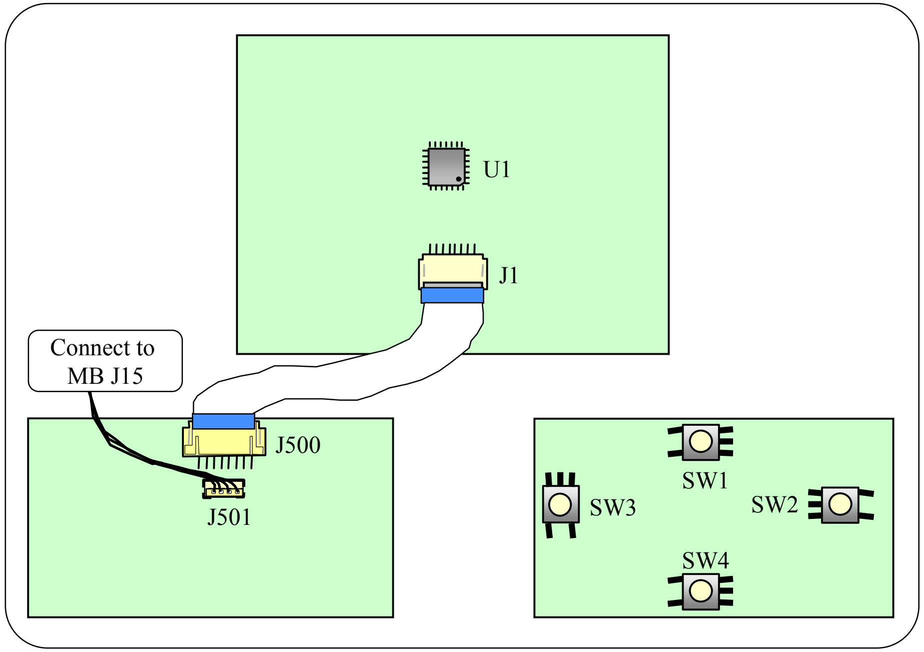
- J1:Parallel port connector
- J2:USB2 connector
- J3:USB0 connector
- J4:TV Out connector
- J5:Power Jack connector
- J6:Inverter Board connector
- PJ1:D/D Board connector
- PJ2: External USB(PIO,IR,TV OUT)Connector



D/D Board Rear Side View

3. Definition & Location Connectors / Switches Setting

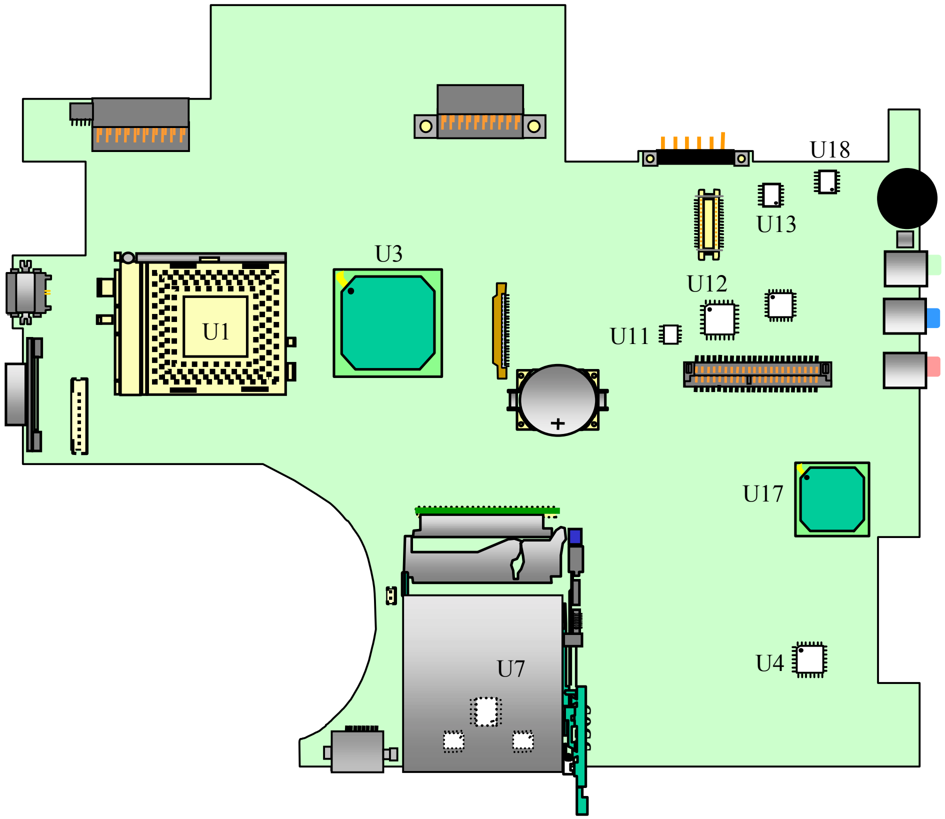
3.3 Touch PAD Board



- SW1:SCRL UP
- SW2:RIGHT
- SW3:LEFT
- SW4:SCRL DOWN
- J501:Touch PAD connector(to MB)

4. Definition & Location Major Components

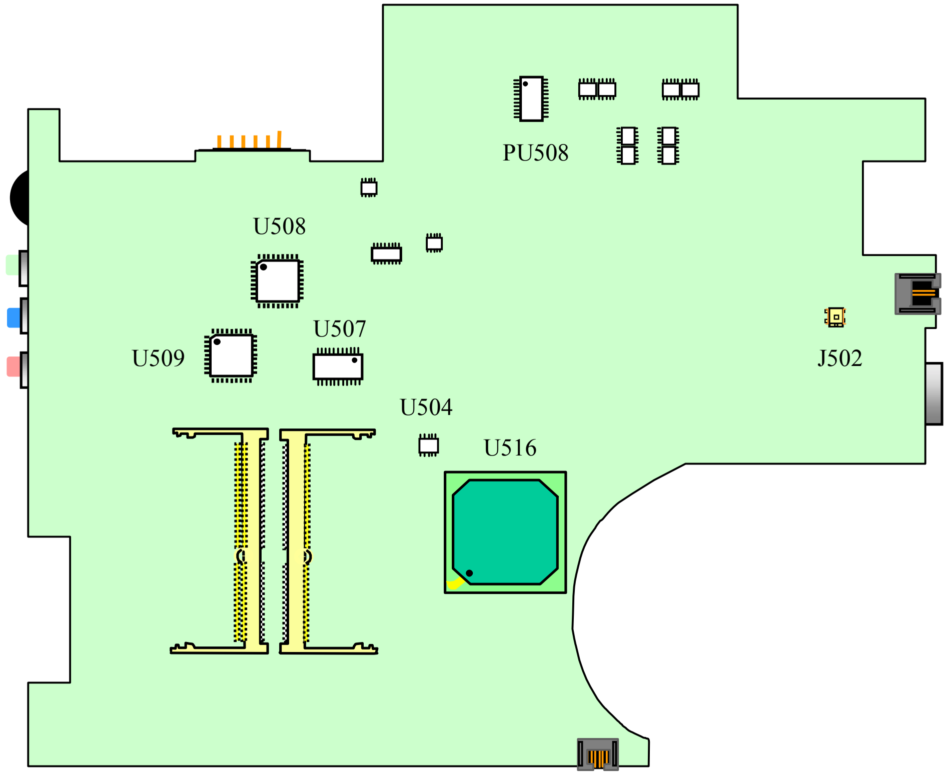
4.1 Main Board (Side A)



- U1:P4(Willamette/Northwood)Micro CPU
- U3:82845 (Memory controller HUB)
- U4:RTL8139CL(LANPHY)
- U7:PCI4410(PCMCIA/1394 controller)
- U11:74AHC373_V
- U12:Flash Rom
- U13:SN74CBTD3384(Level Shift)
- U17:82801BA(I/O controller)
- U18: Audio amplifier

4. Definition & Location Major Components

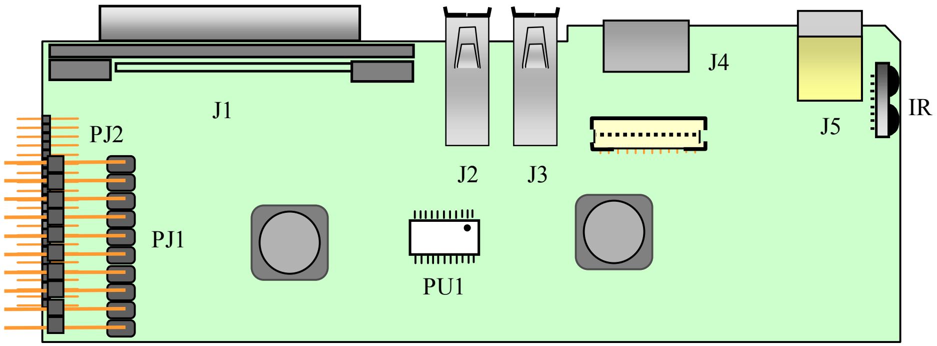
4.1 Main Board (Side B)



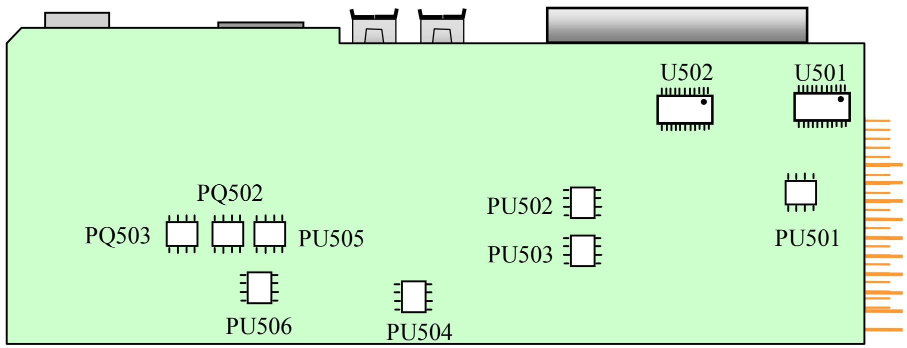
- U504:TPS2211
- U507:ICS950805(Clock generator)
- U508:Micro Controller(H8 F3437)
- U509:PC87393(Supper I/O)
- U516:ATI VGA controller
- PU508:LTC1709EG-9(CPU_CORE regulator)

4. Definition & Location Major Components

4.2 D/D Board



D/D Board (Side A)



D/D Board (Side B)

- U501:PAC128401Q
- U502:PAC128401Q
- PU1:MAX1632(3V.5V.12V regulator)
- PU501:AO4400
- PU502:SI4832DY
- PU503:SI4800DY
- PU504:AO4400
- PU505:SI4832Dy
- PU506:SI4800Y
- PQ502:SI4835DY
- PQ503:SI4835DY

5. Pin Descriptions of Major Components

5.1 Pentium 4(Willamette/Northwood) mFC-PGA2 478 pin

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2 36 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium 4 processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	**ADSTB0#**
A[35:17]#	**ADSTB1#**

Name	Type	Description
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#,A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. The following table defines

Request Signals	subphase 1	subphase 2
A[35:24]#	**AP0#**	**AP1#**
A[23:3]#	**AP1#**	**AP0#**
REQ[4:0]#	**AP1#**	**AP0#**

Name	Type	Description
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V CROSS .
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

5.1 Pentium 4(Willamette/Northwood) mFC-PGA2 478 pin

Name	Type	Description
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Please refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more detailed information. **These signals do not have on-die termination. the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for termination requirements.**
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. **This signal does not have on-die termination and must be terminated.**
BSEL[1:0]	Output	The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Pentium 4 processor in the 478-pin package operates currently at a 400 MHz system bus frequency (100 MHz BCLK[1:0] frequency). For more information about these pins, including termination recommendations.
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for details on implementation.

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#. **Quad-Pumped Signal Groups** (see table below) Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DBI[3:0] Assignment To Data Bus** (see table below)
DBR#	Output	DBR# is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.

Quad-Pumped Signal Groups

Data Group	DSTBN#/ DSTBP#	DBI#
D[15:0]#	**0**	**0**
D[31:16]#	**1**	**1**
D[47:32]#	**2**	**2**
D[63:48]#	**3**	**3**

DBI[3:0] Assignment To Data Bus

Bus Signal	Data Bus Signals
DBI3#	**D[63:48]#**
DBI2#	**D[47:32]#**
DBI1#	**D[31:16]#**
DBI0#	**D[15:0]#**

5.1 Pentium 4(Willamette/Northwood) mFC-PGA2 478 pin

Name	Type	Description
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus isreleased after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.
DP[3:0]#	Input/ Output	DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus gents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe**: D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe**: D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#	Output	FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*-type floating-point error reporting.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 Vcc. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.

Name	Type	Description
HIT# **HITM#**	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signals does not have on-die termination.**
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	The ITPCLKOUT[1:0] pins do not provide any output for the Pentium® 4 processor in the 478-pin package. Refer to
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

5.1 Pentium 4(Willamette/Northwood) mFC-PGA2 478 pin

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled.

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. **This signal does not have on-die termination and must be terminated on the system board.**
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

5.1 Pentium 4(Willamette/Northwood) mFC-PGA2 478 pin

Name	Type	Description
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also knownas the Test Access Port).

Name	Type	Description
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] **TESTHI[5:0]**	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP# , if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.1 Pentium 4(Willamette/Northwood) mFC-PGA2 478 pin

Name	Type	Description
$V_{CCIOPLL}$	Input	$V_{CCIOPLL}$ provides isolated power for internal processor system bus PLLs. Follow he guidelines for V_{CCA}, and refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
$V_{CCSENSE}$	Output	$V_{CCSENSE}$ is an isolated low impedance connection to processor core power(VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	There is no imput voltage requirement for VCCVID for designs intended tosupport only the Pentium 4 processor in the 478-pin package. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (Vcc). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See 1.4 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V_{SSA}	Input	V_{SSA} is the isolated ground for internal PLLs.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.2 Intel 82845(Brookdale Memory Controller HUB)

System Bus singnals

Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O AGTL+	**Block Next Request:** BNR# is used to block the current request bus owner from issuing a new request. This signal dynamically controls the system bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The MCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BR0#	I/O AGTL+	**Bus Request 0#:** The MCH pulls the processor bus BR0# signal low during CPURST#. The signal is sampled by the processor on the active - to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 BCLKs and the maximum hold time is 20 BCLKs. BR0# should be three-stated after the hold time requirement has been satisfied.
CPURST#	O AGTL+	**Processor Reset:** The CPURST# pin is an output from the MCH. The MCH asserts CPURST# while RSTIN# (PCIRST# from the ICH2) is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processor to begin execution in a known state.
DBSY#	I/O AGTL+	**Data Bus Busy:** DBSY# is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer Response:** This signal, when asserted, indicates that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
DBI[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** DBI[3:0]# are driven along with the HD[63:0]# signals. DBI[3:0]# Indicate if the associated data signals are inverted. DBI[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DBI[x]#** — **Data Bits** DBI3# — HD[63:48]# DBI2# — HD[47:32]# DBI1# — HD[31:16]# DBI0# — HD[15:0]#
DRDY#	I/O AGTL+	**Data Ready.** Asserted for each cycle that data is transferred.

Name	Type	Description
HA[31:3]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connect to the system address bus. During processor cycles, HA[31:3]# are inputs. The MCH drives HA[31:3]# during snoop cycles on behalf of the hub interface and AGP/Secondary PCI initiators. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the system bus.
HADSTB[1:0]#	I/O AGTL+	**Host Address Strobe:** The source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** — **Address Bits** HADSTB0# — HA[16:3]#, HREQ[4:0]# HADSTB1# — HA[31:17]#
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the system data bus. HD[63:0]# are transferred at a 4x rate. Note that the data signals are inverted on the system bus.
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes used to transfer HD[63:0]# and DBI[3:0]# at the 4x transfer rate. **Strobe** — **Data Bits** HDSTBP3#, HDSTBN3# — HD[63:48]#, DBI3# HDSTBP2#, HDSTBN2# — HD[47:32]#, DBI2# HDSTBP1#, HDSTBN1# — HD[31:16]#, DBI1# HDSTBP0#, HDSTBN0# — HD[15:0]#, DBI0#
HIT#	I/O AGTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. HIT# is also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. HITM# is also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All system bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., no hub interface or AGP snoopable access to system memory are allowed when HLOCK# is asserted by the processor).

5.2 Intel 82845(Brookdale Memory Controller HUB)

System Bus singnals

Name	Type	Description
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** These signals define the attributes of the request. In Enhanced Mode HREQ[4:0]# are transferred at 2x rate. HREQ[4:0]# are asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the MCH host bridge are defined in the Section 5.1.
HTRDY#	I/O AGTL+	**Host Target Ready:** HTRDY# indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** RS[2:0]# indicates the type of response according to the following table: **RS[2:0]** **Response Type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by MCH) 100 Hard Failure (not driven by MCH) 101 No data response 110 Implicit Write back 111 Normal data response
SCS[11:0]#	O AGTL+	**Chip Select:** These signals select the particular SDRAM components during the active state. **Note:** There are two SCS# signals per SDRAM row. These signals can be toggled on every rising system memory clock edge.
SMA[12:0]	O AGTL+	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to SDRAM.
SBS[1:0]	O AGTL+	**Memory Bank Select:** SBS[1:0] define the banks that are selected within each SDRAM row. The SMA and SBS signals combine to address every possible location in a SDRAM device.
SRAS#	O AGTL+	**SDRAM Row Address Strobe:** SRAS# is Used with SCAS# and SWE# (along with SCS#) to define the DRAM commands.
SCAS#	O AGTL+	**SDRAM Column Address Strobe:** SCAS# is used with SRAS# andSWE# (along with SCS#) to define the SDRAM commands.
SWE#	O AGTL+	**Write Enable:** SWE# is used with SCAS# and SRAS# (along with SCS#) to define the SDRAM commands.
SDQ[63:0]	I/O AGTL+	**Data Lines:** These signals are used to interface to the SDRAM data bus.
SCB[7:0]	I/O AGTL+	**Check Bit Data Lines:** These signals are used to interface to the SDRAM ECC signals.

Name	Type	Description
SCKE[5:0]	O AGTL+	**Clock Enable:** These pins are used to signal a self-refresh or Powerdown command to a SDRAM array when entering system suspend. SCKE is also used to dynamically powerdown inactive SDRAM rows. There is one SCKE per SDRAM row. These signals can be toggled on every rising SCLK edge.
RDCLKO	O AGTL+	**Clock Output:** RDCLKO is used to emulate source-synch clocking for reads. This signal connects to RDCLKIN.
SMA[12:0]	O AGTL+	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to SDRAM.
RDCLKIN	I AGTL+	**Clock Input:** RDCLKIN is used to emulate source-synch clocking for reads. This signal connects to RDCLKO.

5.2 Intel 82845(Brookdale Memory Controller HUB)

Hub Interface Signals

Name	Type	Description
HI_[10:0]	I/O CMOS	**Hub Interface Signals:** Signals used for the hub interface.
HI_STB	I/O CMOS	**Hub Interface Strobe:** One of two differential strobe signals used to transmit or receive packet data over the hub interface.
HI_STB#	I/O CMOS	**Hub Interface Strobe Compliment:** One of two differential strobe signals used to transmit or receive packet data over the hub interface.

AGP Addressing Signals

Name	Type	Description
PIPE#	I AGP	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full-width address is to be enqueued on by the target using the AD bus. One address is placed in the AGP request queue on each rising clock edge while PIPE# is asserted. When PIPE# is deasserted, no new requests are queued across the AD bus. **During SBA Operation:** Not Used. **During FRAME# Operation:** Not Used. PIPE# is a sustained three-state signal from masters (graphics controller), and is an MCH input. **Note:** Initial AGP designs may not use PIPE# (i.e., PCI only 66 MHz). Therefore, an 8 k. pull-up resistor connected to this pin is required on the motherboard.
SBA[7:0]	I AGP	**Sideband Address:** These signals are used by the AGP master (graphics controller) to place addresses into the AGP request queue. The SBA bus and AD bus operate independently. That is, a transaction can proceed on the SBA bus and the AD bus simultaneously. **During PIPE# Operation:** Not Used. **During FRAME# Operation:** Not Used. **Note:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-up resistors are required).

NOTE: The above table contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism but rather a static decision when the device is first being configured after reset.

AGP Flow Control Signals

Name	Type	Description
RBF#	I AGP	**Read Buffer Full:** RBF# indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted, the MCH is not allowed to initiate the return low priority read data. That is, the MCH can finish returning the data for the request currently being serviced. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data, then it is not required to implement this signal. **During FRAME# Operation:** Not Used.
WBF#	I AGP	**Write-Buffer Full:** Indicates if the master is ready to accept fast write data from the MCH. When WBF# is asserted, the MCH is not allowed drive fast write data to the AGP master. WBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data, then it is not required to implement this signal. **During FRAME# Operation:** Not Used.

AGP Status Signals

Name	Type	Description
ST[2:0]	O AGP	**Status:** ST[2:0] provides information from the arbiter to an AGP Master on what it may do. ST[2:0] only have meaning to the master when its G_GNT# is asserted. When G_GNT# is deasserted, these signals have no meaning and must be ignored. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings. **During FRAME# Operation:** These signals are not used during FRAME#-based operation, except that a ¡¥111¡¦ indicates that the master may begin a FRAME# transaction.

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AGP Strobes Signals

Name	Type	Description
AD_STB0	I/O (s/t/s) AGP	**Address/Data Bus Strobe-0:** This signal provides timing for 2x and 4x data on AD[15:0] and the C/BE[1:0]# signals. The agent that is providing the data drives this signal.
AD_STB0#	I/O (s/t/s) AGP	**Address/Data Bus Strobe-0 Compliment:** Differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals. The agent that is providing the data drives this signal.
AD_STB1	I/O (s/t/s) AGP	**Address/Data Bus Strobe-1:** This signal provides timing for 2x- and 4x-clocked data on AD[31:16] and C/BE[3:2]# signals. The agent that is providing the data drives this signal.
AD_STB1#	I/O (s/t/s) AGP	**Address/Data Bus Strobe-1 Compliment:** The differential compliment to the AD_STB1 signal. It is used to provide timing for 4x-clocked data.
SB_STB	I AGP	**Sideband Strobe:** This signal provides timing for 2x- and 4x-clocked data on the SBA[7:0] bus. It is driven by the AGP master after the system has been configured for 2x- or 4x- clocked sideband address delivery.
SB_STB#	I AGP	**Sideband Strobe Compliment:** SB_STB# is the differential compliment to the SB_STB signal. It is used to provide timing for 4x-clocked data.

AGP/PCISignals

For transactions on the AGP interface carried using AGP FRAME# protocol, these signals operate similar to their semantics in the PCI 2.1 specification the exact role of all AGP FRAME# signals are defined below.

Name	Type	Description
G_FRAME#	I/O (s/t/s) AGP	**FRAME:** During FRAME# Operations, G_FRAME# is an output when the MCH acts as an initiator on the AGP Interface.
G_IRDY#	I/O (s/t/s) AGP	**Initiator Ready#:** This signal indicates the AGP compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.
G_TRDY#	I/O (s/t/s) AGP	**Target Ready:** This signal indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
G_STOP#	I/O (s/t/s) AGP	**STOP:** G_STOP Is an input when the MCH acts as a FRAME#-based AGP initiator and an output when the MCH acts as a FRAME#-based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
G_DEVSEL#	I/O (s/t/s) AGP	**Device Select:** This signal indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The MCH asserts G_DEVSEL# based on the DRAM address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
G_REQ#	I AGP	**Request:** Indicates that a FRAME# or PIPE#-based AGP master is requesting use of the AGP interface. This signal is an input into the MCH.
G_GNT#	O AGP	**Grant:** During SBA, PIPE# and FRAME# operation, G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next.
G_AD[31:0]	I/O AGP	**Address/Data Bus:** These signals are used to transfer both address and data on the AGP interface.
G_C/BE[3:0]#	I/O AGP	**Command/Byte Enable:** **During FRAME# Operation:** During the address phase of a transaction, G_C/BE[3:0]# define the bus command. During the data phase, G_C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. **During PIPE# Operation:** When an address is enqueued using PIPE#, the G_C/BE# signals carry command information. The command encoding used during PIPE#-based AGP is DIFFERENT than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus).

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AGP/PCISignals

Name	Type	Description
G_PAR	I/O AGP	**Parity:** **During FRAME# Operations:** This signal is driven by the MCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the MCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across AD[31:0] and G_C/BE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.

Clocks, Reset, and Miscellaneous Signals

Name	Type	Description
BCLK **BCLK#**	I CMOS	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the host clock domain.
66IN	I CMOS	**66 MHz Clock In:** This pin receives a 66 MHz clock from the clock synthesizer. This clock is used by AGP/PCI and hub interface clock domains. **Note:** That this clock input is 3.3 V tolerant.
SCK[11:0]	O CMOS	**System Memory Clocks (SDR):** These signals deliver a synchronized clock to the DIMMs. There are two per row.
RSTIN#	I CMOS	**Reset In:** When asserted, this signal asynchronously resets the MCH logic. RSTIN# is connected to the PCIRST# output of the ICH2. All AGP/PCI output and bi-directional signals will also three-state compliant to PCI Rev 2.0 and 2.1 specifications. **Note:** This input needs to be 3.3 V tolerant.
TESTIN#	I CMOS	**Test Input:** This pin is used for manufacturing and board level test purposes. **Note:** This signal has an internal pull-up resistor.

Voltage Reference and Power Signals

Name	Type	Description
HVREF	Ref	**Host Reference Voltage:** Reference voltage input for the data, address, and common clock signals of the host AGTL+ interface.
SDREF	Ref	**SDRAM Reference Voltage:** Reference voltage input for DQ, DQS, RDCLKIN (SDR).
HI_REF	Ref	**Hub Interface Reference:** Reference voltage input for the hub interface.
AGPREF	Ref	**AGP Reference:** Reference voltage input for the AGP interface.
HLRCOMP	I/O CMOS	**Compensation for Hub Interface:** This signal is used to calibrate the hub interface I/O buffers. It is connected to a 40.2 . pull-up resistor with 1% tolerance and is pulled up to VCC1_8.
GRCOMP	I/O CMOS	**Compensation for AGP:** This signal is used to calibrate buffers. It is connected to a 40.2 . pull-down resistor with a 1% tolerance.
HRCOMP[1:0]	I/O CMOS	**Compensation for Host:** These signals are used to calibrate the host AGTL+ I/O buffers. Each signal is connected to a 24.9 . pull-down resistor with a 1% tolerance.
HSWNG[1:0]	I CMOS	**Host Reference Voltage:** Reference voltage input for the compensation logic.
SMRCOMP	I/O CMOS	**System Memory RCOMP:**
VCC1_5		**1.5 V Power Input:** These pins are connected to a 1.5 V power source.
VCC1_8		**1.8 V Power Input Pins:** These pins are connected to a 1.8 V power source.
VCCSM		**SDRAM Power Input Pins:** These pins are connected to a 3.3 V power source for SDR.
VCCA[1:0]		**PLL Power Input Pins:** These pins provide power for the PLL.
VTT		**AGTL+ Bus Termination Voltage Inputs:** These pins provide the AGTL+ bus termination.
VSS		**Ground:** The VSS pins are the ground pins for the MCH.
VSSA[1:0]		**PLL Ground:** The VSSA[1:0] pins are the ground pins for the PLL on the MCH.

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Hub Interface Signals

Name	Type	Description
HL[11:0]	I/O	**Hub Interface Signals**
HL_STB	I/O	**Hub Interface Strobe:** One of two differential strobe signals used to transmit and receive data through the hub interface.
HL_STB#	I/O	**Hub Interface Strobe Complement:** Second of the two differential strobe signals.
HLCOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.

LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	**LAN Interface Clock:** This signal is driven by the LAN Connect component. The frequency range is 0.8 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Clock:** EE_SHCLK is the serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data In:** EE_DIN transfers data from the EEPROM to the ICH2. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Out:** EE_DOUT transfers data from the ICH2 to the EEPROM.
EE_CS	O	**EEPROM Chip Select:** EE_CS is a chip-select signal to the EEPROM.

Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / **LAD[3:0]**	I/O	**Firmware Hub Signals:** These signals are muxed with LPC address signals.
FWH[4] / **LFRAME#**	I/O	**Firmware Hub Signals:** This signal is muxed with LPC LFRAME# signal.

PCI Interface Signals

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH2 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction,C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# — Command Type** 0000 — Interrupt Acknowledge 0001 — Special Cycle 0010 — I/O Read 0011 — I/O Write 0110 — Memory Read 0111 — Memory Write 1010 — Configuration Read 1011 — Configuration Write 1100 — Memory Read Multiple 1110 — Memory Read Line 1111 — Memory Write and Invalidate All command encodings not shown are reserved. The ICH2 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH2 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH2 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH2 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH2- initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH2 until driven by a target device.

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PCI Interface Signals

Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH2 when the ICH2 is the target, and FRAME# is an output from the ICH2 when the ICH2 is the Initiator. FRAME# remains tri-stated by the ICH2 until driven by an Initiator.
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH2's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH2 has valid data present on AD[31:0]. During a read, it indicates the ICH2 is prepared to latch data. IRDY# is an input to the ICH2 when the ICH2 is the Target and an output from the ICH2 when the ICH2 is an Initiator. IRDY# remains tri-stated by the ICH2 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH2's ability as a Target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH2, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH2, as a Target is prepared to latch data. TRDY# is an input to the ICH2 when the ICH2 is the Initiator and an output from the ICH2 when the ICH2 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH2 until driven by a target.
STOP#	I/O	**Stop:** STOP# indicates that the ICH2, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH2, as an Initiatior, to stop the current transaction. STOP# is an output when the ICH2 is a target and an input when the ICH2 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH2.
REQ[0:4]# REQ[5]# / REQ[B]# / GPIO[1]	I	**PCI Requests:** The ICH2 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. Note: REQ[0]# is programmable to have improved arbitration latency for supporting PCI-based 1394 controllers.

Name	Type	Description
PAR	I/O	**Calculated/Checked Parity:** PAR uses "even" parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. "Even" parity means that the ICH2 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH2 always calculates PAR on 36 bits, regardless of the valid byte enables. The ICH2 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH2 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH2 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH2 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH2 is the Initiator of a PCI write transaction, and when it is the target of a read transaction. ICH2 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH2 sets the appropriate internal status bits, and has the option to generate an NMI# or SMI#.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH2 drives PERR# when it detects a parity error. The ICH can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
GNT[0:4]# GNT[5]# / GNT[B]# / GPIO[17]#	O	**PCI Grants:** The ICH2 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pullups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pullup.
PCICLK	I	**PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. . Note:For 82801BAM ICH2-M, this clock does not stop based on the STP_PCI# signal. The PCI Clock only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	**PCI Reset:** ICH2 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH2 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH2 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH2 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
SERR#	I	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH2 has the ability to generate an NMI, SMI#, or interrupt.

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PCI Interface Signals

Name	Type	Description
PME#	I	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate SCI from the S0 state. In some cases the ICH2 may drive PME# active due to an internal wake event. The ICH2 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN# (ICH2-M only)	I/O	**PCI Clock Run:** For the ICH2-M, CLKRUN# is used to support PCI Clock Run protocol. This signal connects to PCI devices that need to request clock re-start or prevention of clock stopping.
REQ[A]# / GPIO[0] REQ[B]# / REQ[5]# / GPIO[1]	I	**PC/PCI DMA Request [A:B]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI-based Super I/O or audio codecs that need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. Instead, REQ[B]# can be used as the 6th PCI bus request.
GNT[A]# / GPIO[16] GNT[B]# / GNT[5]# / GPIO[17]	O	**PC/PCI DMA Acknowledges [A:B]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA master cycles over the PCI bus. This is used by devices such as PCI-based Super/IO or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Name	Type	Description
PDCS1#, SDCS1#	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** These signals are for the ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** These signals are for the ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.

IDE Interface Signals(continued)

Name	Type	Description
PDA[2:0], SDA[2:0]	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.
PDD[15:0], SDD[15:0]	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, SDDREQ	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. They are not associated with any AT-compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, SDDACK#	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each signal is asserted by the ICH2 to indicate to the IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR# SDIOR#	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data on the PDD or SDD lines. Data is latched by the ICH2 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). **Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk):** This is the data write strobe for writes to disk. When writing to disk, ICH2 drives valid data on rising and falling edges of PDWSTB or SDWSTB. **Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk):** This is the DMA ready for reads from disk. When reading from disk, ICH2 deasserts PRDMARDY# orSRDMARDY# to pause burst data transfers.

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IDE Interface Signals(continued)

Name	Type	Description
PDIOW# **SDIOW#**	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). **Primary and Secondary Disk Stop (Ultra DMA):** ICH2 asserts this signal to terminate a burst.
PIORDY **SIORDY**	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal keeps the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. **Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk)**: When reading from disk, ICH2 latches data on rising and falling edges of this signal from the disk. **Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk)**: When writing to disk, this is deasserted by the disk to pause burst data transfers

USB Interface Signals

Name	Type	Description
USBP0P, **USBP0N,** **USBP1P,** **USBP1N**	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1 (USB Controller 1).
USBP2P, **USBP2N,** **USBP3P,** **USBP3N**	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 2 and 3 USB Controller 2).
OC[3:0]#	I	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.

Interrupt Signals

Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3:7, 9:12, 14, or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the ISA interrupts.
PIRQ[H]#, **PIRQ[G:F]#** **GPIO[4:3],** **PIRQ[E]#**	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3:7, 9:12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the ISA interrupts. If not needed for interrupts, PIRQ[G:F] can be used as GPIO.
IRQ[14:15]	I	**Interrupt Request 14:15:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the primary controller and IRQ15 is used by the drives connected to the secondary controller.
APICCLK	I	**APIC Clock:** The APIC clock runs at 33.333 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs, the data is valid on the rising edge of APICCLK.As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** Internal pull-ups are provided.
LFRAME# / FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	O	**LPC Serial DMA/Master Request Inputs:** These signals are used to request DMA or bus master access. Typically, they are connected to external Super I/O device. An internal pull-up resistor is provided on these signals.

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Power Management Interface Signals

Name	Type	Description
THRM#	I	**Thermal Alarm:** THRM# is an active low signal generated by external hardware to start the hardware clock throttling mode. This signal can also generate an SMI# or an SCI.
SLP_S1# (ICH2-M only)	O	**S1 Sleep Control:** Clock synthesizer or power plane control. This signal connects to clock synthesizer's PWRDWN# signal. An optional use is to shut off power to non-critical systems when in the S1 (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S3#	O	**S3 Sleep Control:** Power plane control. This signal is used to shut off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S5#	O	**S5 Sleep Control:** Power plane control. This signal is used to shut power off to all non-critical systems when in the S4 (Suspend To Disk) or S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH2 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH2 asserts PCIRST#.
RSM_PWROK (ICH2 0nly)	I	**Resume Well Power OK:** When asserted, this signal is an indication to the ICH2 that the resume well power (VccSus3_3, VccSus1_8) has been stable for at least10 ms.
LAN_PWROK (ICH2-M only)	I	**LAN Power OK:** When asserted, this signal is an indication to the ICH2-M that the LAN Controller power (VccLAN3_3, VccLAN1_8) has been stable for at least 10 ms.
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override will occur even if the system is in the S1-S4 states. This signal has an internal pull-up resistor.
RI#	I	**Ring Indicate:** From the modem interface. This signal can be enabled as a wake event; this is preserved across power failures.
RSMRST#	I	**Resume Well Reset:** RSMRST# is used for resetting the resume power plane logic.
SUS_STAT# / LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH2 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC interface.

Name	Type	Description
C3_STAT# / GPIO[21] ICH2-M only)	O	**C3_STAT#:** This ICH2-M signal is typically configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal can be used as a GPO.
SUSCLK	O	**Suspend Clock:** This signal is an output of the RTC generator circuit and is used by other chips for the refresh clock.
VRMPWRGD (ICH2) VRMPWRGD/ VGATE (ICH2-M)	I	**VRM Power Good (ICH2 and ICH2-M):** VRMPWRGD should be connected to be the processor's VRM Power Good.
VGATE / **VRMPWRGD (ICH2-M only)**	I	**VRM Power Good Gate (ICH2-M):** VGATE is used for Intel® SpeedStepTM technology support. It is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal can go inactive during a Intel® SpeedStepTM transition. In non-Intel® SpeedStepTM technology systems this signal should be connected to the processor VRM Power Good.
AGPBUSY# (ICH2-M only)	I	**AGP Bus Busy:** This signal supports the C3 state. It provides an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI# (ICH2-M only)	O	**Stop PCI Clock:** This signal is an output to the external clock generator to turn off the PCI clock. It is used to support PCI CLKRUN# protocol. If this functionality is not needed, this signal can be configured as a GPO.
STP_CPU# (ICH2-M only)	O	**Stop CPU Clock:** Output to the external clock generator to turn off the processor clock. It is used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW# (ICH2-M only)	I	**Battery Low:** Input from battery to indicate that there is insufficient power to boot the system. Assertion prevents wake from S1–S5 state. This signal can also be enabled to cause an SMI# when asserted. In desktop configurations this signal should be pulled high to VccSUS.
CPUPERF# (ICH2-M only)	OD	**CPU Performance:** This signal is used for Intel® SpeedStepTM technology support. It selects which power state to put the processo in. If this functionality is not needed, this signal can be configured as a GPO. This is an open-drain output signal and requires an external pull-up to the processor I/O voltage.
SSMUXSEL (ICH2-M only)	O	**SpeedStep Mux Select:** This signal is used for Intel SpeedStepTM technology support. It selects the voltage level for the processor. If this functionality is not needed, this signal can be configured as a GPO.

5.3 Intel 82801BA(I/O Controller HUB)

Processor Interface Signals

Name	Type	Description
A20M#	O	**Mask A20:** A20M# goes active based on setting the appropriate bit in the Port 92h register, or based on the A20GATE signal. **Speed Strap:** During the reset sequence, ICH2 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	**Processor Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH2 can optionally assert the CPUSLP# signal when going to the S1 state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH2 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH2 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH2 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH2 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	**Initialization:** INIT# is asserted by the ICH2 for 16 PCI clocks to reset the processor. ICH2 can be configured to support processor BIST. In that case, INIT# will be active when PCIRST# is active.
INTR	O	**Processor Interrupt:** INTR is asserted by the ICH2 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH2 drives INTR high if the corresponding bit is set in the FREQ_STRP register.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The ICH2 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH2 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH2 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH2 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset Processor:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH2's other sources of INIT#. When the ICH2 detects the assertion of this signal, INIT# isgenerated for 16 PCI clocks.. **Note:** 82801BA ICH2: The 82801BA ignores RCIN# assertion during transitions to the S3, S4 and S5 states. 82801BAM ICH2-M: The 82801BAM ignores RCIN# assertion during transitions to the S1, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** This signal is from the keyboard controller. It acts as an alternative method to force the A20M# signal active. A20GATE saves the external OR gate needed with various other PCIsets.
CPUPWRGD	OD	**CPU Power Good (82801BAM ICH2-M):** This signal should be connected to the processor's PWRGOOD input. For Intel® SpeedStep™ technology support, this signal is kept high during a Intel® SpeedStep™ technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH2-M's PWROK and VGATE / VRMPWRGD signals.

SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate an SMI#. If not used for SMBALERT#, it can be used as a GPI.

5.3 Intel 82801BA(I/O Controller HUB)

System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** These signals are an SMBus link to an optional external system management ASIC or LAN controller. External pull-ups are required. **Note:** that SMLINK[0] corresponds to an SMBus Clock signal and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX2 should be left floating.

Other Clocks

Name	Type	Description
CLK14	I	**Oscillator Clock:** CLK14 is used for 8254 timers and runs at 14.31818 MHz. **82801BA ICH2:** This clock is permitted to stop during S3 (or lower) states. **82801BAM ICH2-M:** This clock is permitted to stop during S1 (or lower) states.
CLK48	I	**48 MHz Clock:** CLK48 is used to for the USB controller and runs at 48 MHz. **82801BA ICH2:** This clock is permitted to stop during S3 (or lower) states. **82801BAM ICH2-M:** This clock is permitted to stop during S1 (or lower) states.
CLK66	I	**66 MHz Clock:** CLK66 is used to for the hub interface and runs at 66 MHz. **82801BA ICH2:** This clock is permitted to stop during S3 (or lower) states. **82801BAM ICH2-M:** This clock is permitted to stop during S1 (or lower) states.

Miscellaneous Signals

Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 1. **Note:** SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 register). **Note:** Clearing CMOS in an ICH2-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
TP0 (ICH2 0nly)	I	**Test Point (82801BA ICH2):** This signal must have an external pull-up to VccSus3_3.
FS0	I	**Functional Strap:** This signal is reserved for future use. There is an internal pullup resistor on this signal.

AC'97 Link Signals

Name	Type	Description
AC_RST#	O	**AC97 Reset:** Master H/W reset to external Codec(s)
AC_SYNC	O	**AC97 Sync:** 48 KHz fixed rate sample sync to the Codec(s)
AC_BIT_CLK	I	**AC97 Bit Clock:** 12.288 MHz serial data clock generated by the external Codec(s). See Note.
AC_SDOUT	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s) **Note:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap..
AC_SDIN[1:0]	I	**AC97 Serial Data In 0:** Serial TDM data inputs from the Codecs. See Note.

5.4 PCI4410(PCMCIA/1394 LINK Controller)

Power-Supply Terminals

Name	Type	Description
GND		Device ground terminals
VCC		Power-supply terminal for core logic (3.3 V)
VCCB		Clamp voltage for PC Card interface. Matches card signaling environment, 5 V or 3.3 V.
VCCI		Clamp voltage for miscellaneous I/O signals (MFUNC, GRST#, and SUSPEND#)
VCCL		Clamp voltage for 1394 link function
VCCP		Clamp voltage for PCI interface, ZV interface, SPKROUT, INTA#, INTB# LED_SKT,VCCD0#, VCCD1#, VPPD0, VPPD1

PC Card Power-Switch Terminals

Name	Type	Description
VCCD0# **VCCD1#**	O	Logic controls to the TPS2211 PC Card power-switch interface to control AVCC
VPPD0 **VPPD1**	O	Logic controls to the TPS2211 PC Card power-switch interface to control AVPP

PCI System Terminals

Name	Type	Description
GRST#	I	Global reset. When global reset is asserted, GRST# causes the PCI4410A device to place all output buffers in a high-impedance state and reset all internal registers. When GRST# is asserted, the device is completely in its default state. For systems that require wake-up from D3, GRST# normally is asserted only during initial boot. PRST# should be asserted following initial boot so that PME context is retained when transitioning from D3 to D0. For systems that do not require wake-up from D3, GRST# should be tied to PRST. When the SUSPEND mode is enabled, the device is protected from GRST#, and the internal registers are preserved. All outputs are placed in a high-impedance state, but the contents of the registers are preserved.
PCLK	I	PCI bus clock. PCLK provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
PRST#	I	PCI bus reset. When the PCI bus reset is asserted, PRST# causes the PCI4410A device to place all output buffers in a high-impedance state and reset internal registers. When PRST is asserted, the device is completely nonfunctional. After PRST# is deserted, the PCI4410A device is in a default state. When SUSPEND# and PRST# are asserted, the device is protected from PRST# clearing the internal registers.All outputs are placed in a high-impedance state, but the contents of the registers are preserved.

PCI Address and Data Terminals

Name	Type	Description
AD[0:31[	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
C/BE[0:3]#	I/O	PCI bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, C/BE3#–C/BE0# define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. C/BE0# applies to byte 0 (AD7–AD0), C/BE1# applies to byte 1 (AD15–AD8), C/BE2# applies to byte 2 (AD23–AD16), and C/BE3# applies to byte 3 (AD31–AD24).
PAR	I/O	PCI bus parity. In all PCI bus read and write cycles, the PCI4410A device calculates even parity across the AD31–AD0 and C/BE3#–C/BE0# buses. As an initiator during PCI cycles, the PCI4410A device outputs this parity indicator with a one-PCLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator’s parity indicator. A compare error results in the assertion of a parity error (PERR#).

PCI Interface Control Terminals

Name	Type	Description
DECSEL#	I/O	PCI device select. The PCI4410A device asserts DEVSEL# to claim a PCI cycle as the target device. As a PCI initiator on the bus, the PCI4410A device monitors DEVSEL# until a target responds. If no target responds before timeout occurs, the PCI4410A device terminates the cycle with an initiator abort.
FRAME#	I/O	PCI cycle frame. FRAME# is driven by the initiator of a bus cycle. FRAME# is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When FRAME# is deasserted, the PCI bus transaction is in the final data phase.
GNT#	I	PCI bus grant. GNT# is driven by the PCI bus arbiter to grant the PCI4410A device access to the PCI bus after the current data transaction has completed. GNT# may or may not follow a PCI bus request, depending on the PCI bus parking algorithm.
IDSEL#	I	Initialization device select. IDSEL# selects the PCI4410A device during configuration space accesses. IDSEL# can be connected to one of the upper 24 PCI address lines on the PCI bus.

5.4 PCI4410(PCMCIA/1394 LINK Controller)

PCI Interface Control Terminals

Name	Type	Description
IRDY#	I/O	PCI initiator ready. IRDY# indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK, when both IRDY# and TRDY# are asserted. Until IRDY# and TRDY# are both sampled asserted, wait states are inserted.
PERR#	I/O	PCI parity error indicator. PERR# is driven by a PCI device to indicate that calculated parity does not match PAR when PERR# is enabled through bit 6 (PERR_EN) of the command register (PCI offset 04h, see Section 4.4).
REQ#	O	PCI bus request. REQ# is asserted by the PCI4410A device to request access to the PCI bus as an initiator.
SERR#	O	PCI system error. SERR# is an output that is pulsed from the PCI4410A device when enabled through bit 8 (SERR_EN) of the command register (PCI offset 04h, see Section 4.4) indicating a system error has occurred. The PCI4410A device need not be the target of the PCI cycle to assert this signal. When SERR# is enabled in the command register, this signal also pulses, indicating that an address parity error has occurred on a CardBus interface.
STOP#	I/O	PCI cycle stop signal. STOP# is driven by a PCI target to request the initiator to stop the current PCI bus transaction. STOP# is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.
TRDY#	I/O	PCI target ready. TRDY# indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK, when both IRDY# and TRDY# are asserted. Until both IRDY# and TRDY# are asserted, wait states are inserted.

Multifunction and Miscellaneous Terminals

Name	Type	Description
INTA#	O	Parallel PCI interrupt. INTA#
INTB#	O	Parallel PCI interrupt. INTB#
LED_SKT	O	PC Card socket activity LED indicator. LED_SKT provides an output indicating PC Card socket activity.
MFUNC0	I/O	Multifunction terminal 0. MFUNC0 can be configured as parallel PCI interrupt INTA#, GPI0, GPO0, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ. See Section 4.32, Multifunction Routing Register, for configuration details.

Name	Type	Description
MFUNC1	I/O	Multifunction terminal 1. MFUNC1 can be configured as GPI1, GPO1, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ. See Section 4.32, Multifunction Routing Register, for configuration details. Serial data (SDA). When VCCD0# and VCCD1# are high after a PCI reset, the MFUNC1 terminal provides the SDA signaling for the serial bus interface. The two-terminal serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset. See Section 3.6.1, Serial Bus Interface Implementation, for details on other serial bus applications.
MFUNC2	I/O	Multifunction terminal 2. MFUNC2 can be configured as PC/PCI DMA request, GPI2, GPO2, ZV switching outputs, CardBus audio PWM, GPE#, RI_OUT#, or a parallel IRQ. See Section 4.32, Multifunction Routing Register, for configuration details.
MFUNC3	I/O	Multifunction terminal 3. MFUNC3 can be configured as a parallel IRQ or the serialized interrupt signal IRQSER. See Section 4.32, Multifunction Routing Register, for configuration details.
MFUNC4	I/O	Multifunction terminal 4. MFUNC4 can be configured as PCI LOCK#, GPI3, GPO3, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, RI_OUT#, or a parallel IRQ. See Section 4.32, Multifunction Routing Register, for configuration details. Serial clock (SCL). When VCCD0# and VCCD1# are high after a PCI reset, the MFUNC4 terminal provides the SCL signaling for the serial bus interface. The two-terminal serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset. See Section 3.6.1, Serial Bus Interface Implementation, for details on other serial bus applications.
MFUNC5	I/O	Multifunction terminal 5. MFUNC5 can be configured as PC/PCI DMA grant, GPI4, GPO4, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ. See Section 4.32, Multifunction Routing Register, for configuration details.
MFUNC6	I/O	Multifunction terminal 6. MFUNC6 can be configured as a PCI CLKRUN# or a parallel IRQ. See Section 4.32, Multifunction Routing Register, for configuration details.
RI_OUT#/PME#	O	Ring indicate out and power-management event output. Terminal provides an output for ring-indicate or PME# signals.
SPKROUT	O	Speaker output. SPKROUT is the output to the host system that can carry SPKR# or CAUDIO through the PCI4410A device from the PC Card interface. SPKROUT is driven as the exclusive-OR combination of card SPKR#//CAUDIO inputs.
SUSPEND#	I	Suspend. SUSPEND# protects the internal registers from clearing when the GRST or PRST signal is asserted. See Section 3.8.4, Suspend Mode, for details.

5.4 PCI4410(PCMCIA/1394 LINK Controller)

16-Bit PC Card Address and Data Terminals

Name	Type	Description
ADDR[0:25]	O	PC Card address. 16-bit PC Card address lines. ADDR25 is the most significant bit
DATA[0:15]	I/O	PC Card data. 16-bit PC Card data lines. DATA15 is the most significant bit.

16-Bit PC Card Interface Control Terminals

Name	Type	Description
BVD1 (STSCHG#/RI#)	I	Battery voltage detect 1. BVD1 is generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See Section 5.6, ExCA Card Status-Change-Interrupt Configuration Register, for enable bits. See Section 5.5, ExCA Card Status-Change Register, and Section 5.2,ExCA Interface Status Register, for the status bits for this signal. Status change. STSCHG# is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring indicate. R# is used by 16-bit modem cards to indicate a ring detection.
BVD2 (SPKR#)	I	Battery voltage detect 2. BVD2 is generated by 16-bit memory PC Cards that include batteries. BVD2is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See Section 5.6, ExCA Card Status-Change-Interrupt Configuration Register, for enable bits. See Section 5.5, ExCA Card Status-Change Register, and Section 5.2, ExCA Interface Status Register, for the status bits for this signal. Speaker. SPKR# is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B are combined by the PCI4410A device and are output on SPKROUT.DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts BVD2 to indicate a request for a DMA operation.
CD1# CD2#	I	**Card detect 1** and **Card detect 2**. CD1# and CD2# are connected internally to ground on the PC Card. When a PC Card is inserted into a socket, CD1# and CD2# are pulled low. For signal status, see Section 5.2, ExCA Interface Status Register.

Name	Type	Description
CE1# CE2#	O	**Card enable 1** and **card enable 2**. CE1# and CE2# enable even- and odd-numbered address bytes. CE1#enables even-numbered address bytes, and CE2# enables odd-numbered address bytes.
INPACK#	I	**Input acknowledge**. INPACK# is asserted by the PC Card when it can respond to an I/O read cycle at the current address.DMA request. INPACK# can be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If it is used as a strobe, the PC Card asserts this signal to indicate a request for a DMA operation.
IORD#	O	**I/O read**. IORD# is asserted by the PCI4410A device to enable 16-bit I/O PC Card data output during host I/O read cycles. DMA write. IORD# is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI4410A device asserts IORD# during DMA transfers from the PC Card to host memory.
IOWR#	O	**I/O write**. IOWR# is driven low by the PCI4410A device to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. DMA read. IOWR# is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI4410A device asserts IOWR during transfers from host memory to the PC Card.
OE#	O	**Output enable**. OE# is driven low by the PCI4410A device to enable 16-bit memory PC Card data output during host memory read cycles. DMA terminal count. OE# is used as terminal count (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI4410A device asserts OE# to indicate TC for a DMA write operation.
READ IREQ#	I	**Ready**. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicatethat the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data-transfer command. Interrupt request. IREQ# is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I /O PC Card requires service by the host software. IREQ# is high (deasserted) when no interrupt is requested.

5.4 PCI4410(PCMCIA/1394 LINK Controller)

16-Bit PC Card Interface Control Terminals

Name	Type	Description
REG#	O	**Attribute memory select**. REG# remains high for all common memory accesses. When REG# is asserted, access is limited to attribute memory (OE# or WE# active) and to the I/O space (IORD# or IOWR# active). Attribute memory is a separately accessed section of card memory and generally is used to record card capacity and other configuration and attribute information. DMA acknowledge. REG is used as a DMA acknowledge (DACK#) during DMA operations to a 16-bit PC Card that supports DMA. The PCI4410A device asserts REG# to indicate a DMA operation. REG# is used in conjunction with the DMA read (IOWR#) or DMA write (IORD#) strobes to transfer data.
RESET	O	**PC Card reset**. RESET forces a hard reset to a 16-bit PC Card.
WAIT#	I	**Bus cycle wait**. WAIT# is driven by a 16-bit PC Card to extend the completion of the memory or I/O cycle in progress.
WE#	O	**Write enable**. WE# is used to strobe memory write data into 16-bit memory PC Cards. WE# also is used for memory PC Cards that employ programmable memory technologies. DMA terminal count. WE# is used as TC during DMA operations to a 16-bit PC Card that supports DMA. The PCI4410A device asserts WE to indicate TC for a DMA read operation.
WP **IOIS16#**	I	**Write protect**. WP applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O PC cards, WP is used for the 16-bit port (IOIS16#) function. I/O is 16 bits. IOIS16# applies to 16-bit I/O PC Cards. IOIS16# is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses. DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, the PC Card asserts WP to indicate a request for a DMA operation.
VS1# **VS2#**	I/O	**Voltage sense 1** and **voltage sense 2**. VS1 and VS2, when used in conjunction with each other, determine the operating voltage of the PC Card.

CardBus PC Card Interface System Terminals

Name	Type	Description
CCLK	O	**CardBus clock**. CCLK provides synchronous timing for all transactions on the CardBus interface. All signals except CRST#, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD2#, CCD1#, CVS2, and CVS1 are sampled on the rising edge of CCLK, and all timing parameters are defined with the rising edge of this signal. CCLK operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings.
CCLKRUN#	I/O	**CardBus clock run**. CCLKRUN# is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI4410A device to indicate that the CCLK frequency is going to be decreased.
CRST#	O	**CardBus reset**. CRST# brings CardBus PC Card-specific registers, sequencers, and signals to a known state. When CRST# is asserted, all CardBus PC Card signals are placed in a high-impedance state, and the PCI4410A device drives these signals to a valid logic level. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.

CardBus PC Card Address and Data Terminals

Name	Type	Description
CAD[0:31]	I/O	**CardBus address and data**. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31–CAD0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31–CAD0 contain data. CAD31 is the most significant bit.
CC/BE[0:3]#	I/O	**CardBus bus commands and byte enables**. CC/BE3#–CC/BE0# are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/BE3#–CC/BE0# define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/BE0# applies to byte 0 (CAD7–CAD0), CC/BE1# applies to byte 1 (CAD15–CAD8), CC/BE2# applies to byte 2 (CAD23–CAD16), and CC/BE3# applies to byte 3 (CAD31–CAD24).
CPAR	I/O	**CardBus parity**. In all CardBus read and write cycles, the PCI4410A device calculates even parity across the CAD and CC/BE buses. As an initiator during CardBus cycles, the PCI4410A device outputs CPAR with a one-CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a compare error results in a parity-error assertion.

5.4 PCI4410(PCMCIA/1394 LINK Controller)

CardBus PC Card Interface Control Terminals

Name	Type	Description
CAUDIO	I	**CardBus audio**. CAUDIO is a digital input signal from a PC Card to the system speaker. The PCI4410A device supports the binary audio mode and outputs a binary signal from the card to SPKROUT.
CBLOCK#	I/O	**CardBus lock**. CBLOCK# is used to gain exclusive access to a target.
CCD1# **CCD2#**	I	**CardBus detect 1** and **CardBus detect 2**. CCD1# and CCD2# are used in conjunction with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the operating voltage and card type.
CDEVSEL#	I/O	**CardBus device select**. The PCI4410A device asserts CDEVSEL# to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI4410A device monitors CDEVSEL# until a target responds. If no target responds before timeout occurs, the PCI4410A device terminates the cycle with an initiator abort.
CFRAME#	I/O	**CardBus cycle frame**. CFRAME# is driven by the initiator of a CardBus bus cycle. CFRAME# is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When CFRAME# is deasserted, the CardBus bus transaction is in the final data phase.
CGNT#	O	**CardBus bus grant**. CGNT# is driven by the PCI4410A device to grant a CardBus PC Card access the CardBus bus after the current data transaction has been completed.
CINT#	I	**CardBus interrupt**. CINT# is asserted low by a CardBus PC Card to request interrupt servicing from the host.
CIRDY#	I/O	**CardBus initiator ready**. CIRDY indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK when both CIRDY and CTRDY are asserted. Until both CIRDY and CTRDY are sampled asserted, wait states are inserted.
CPERR#	I/O	**CardBus parity error**. CPERR# reports parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.
CREQ#	I	**CardBus request**. CREQ# indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator.
CSERR#	I	**CardBus system error**. CSERR# reports address parity errors and other system errors that could lead to catastrophic results. CSERR# is driven by the card synchronous to CCLK, but deasserted by a weak pull up, and may take several CCLK periods. The PCI4410A device can report CSERR# to the system by assertion of SERR# on the PCI interface.
CSTOP#	I/O	**CardBus stop**. CSTOP# is driven by a CardBus target to request the initiator to stop the current CardBus transaction. CSTOP# is used for target disconnects, and is commonly asserted by target devices do not support burst data transfers.
CSTSCHG#	I	**CardBus status change**. CSTSCHG alerts the system to a change in the card's status, and is used a wake-up mechanism.
CTRDY#	I/O	**CardBus target ready**. CTRDY# indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK, when both CIRDY and CTRDY# are asserted; until this time, wait states are inserted.
CVS1 **CVS2**		**CardBus voltage sense 1** and **CardBus voltage sense 2**. CVS1 and CVS2 are used in conjunction with CCD1# and CCD2# to identify card insertion and interrogate cards to determine the operating voltage and card type.

IEEE 1394 PHY/Link Interface Terminals

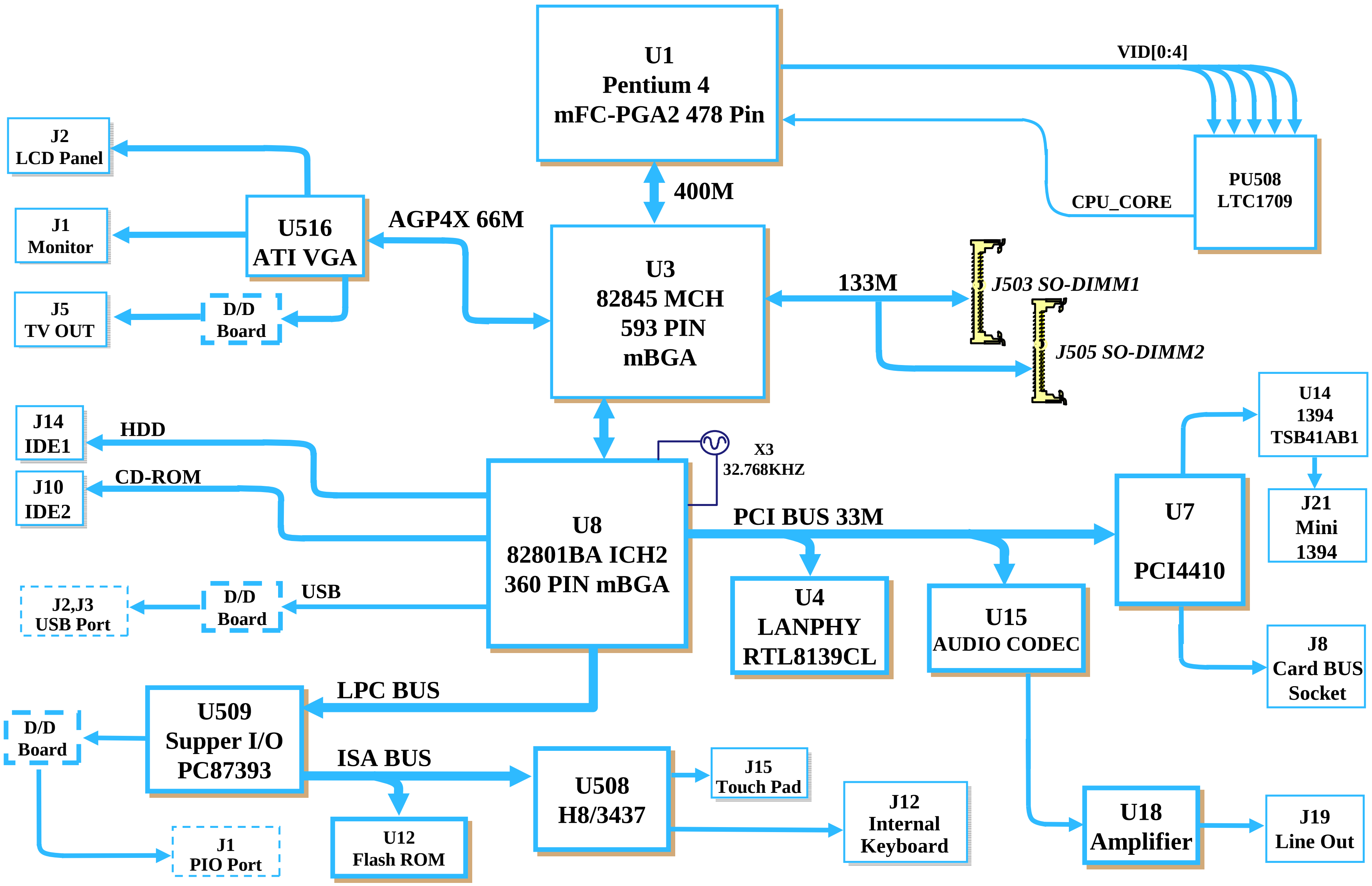
Name	Type	Description
PHY_CTL1 **PHY_CTL0**	I/O	**PHY-link interface control**. These bidirectional signals control passage of information between the PHY and link. The link can drive these terminals only after the PHY has granted permission, following a link request (LREQ).
PHY_DATA[0:7]	I/O	**PHY-link interface data**. These bidirectional signals pass data between the PHY and link. These terminals are driven by the link on transmissions and are driven by the PHY on receptions. Only DATA1–DATA0 are valid for 100-Mbit speed. DATA4–DATA0 are valid for 200-Mbit speed and DATA7–DATA0 are valid for 400-Mbit speed.
PHY_CLK	I	**System clock**. This input provides a 49.152-MHz clock signal for data synchronization.
PHY_REQ	O	**Link request**. This signal is driven by the link to initiate a request for the PHY to perform some service.
LINKON	I	**1394 link on**. This input from the PHY indicates that the link should turn on.
LPS	O	**Link power status**. LPS indicates that link is powered and fully functional.

5.4 PCI4410(PCMCIA/1394 LINK Controller)

Zoomed-Video Interface Terminals

Name	Type	Description
ZV_HREF	O	Horizontal sync to the zoomed-video port
ZV_VSYHC	O	Vertical sync to the zoomed-video port
ZV_Y[0:7]	O	Video data to the zoomed-video port in YUV:4:2:2 format
ZV_UV[0:7]	O	Video data to the zoomed-video port in YUV:4:2:2 format
ZV_SCLK	O	Audio SCLK PCM
ZV_MCLK	O	Audio MCLK PCM
ZV_PCLK	IO	Pixel clock to the zoomed-video port
ZV_LRCLK	O	Audio LRCLK PCM
ZV-SDATA	O	Audio SDATA PCM

6. System Block Diagram



7. Maintenance Diagnostic

7.1 Introduction

Every time the computer is turned on ,the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic post (378H) is written at the beginning of the test. Therefore , if the test fail, the user can determine where the problem occurs by reading the last value written to post 378H by the PIO debug board plug at PIO port.

7.2 Error codes :

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Sizememory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Signon messages displayed

7.2 Error codes :

Following is a list of error codes in sequent display on the PIO debug board.

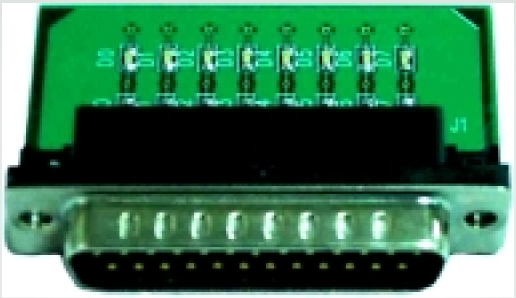
Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code

7.3 Debug Card

7.3.1 Diagnostic Tools :

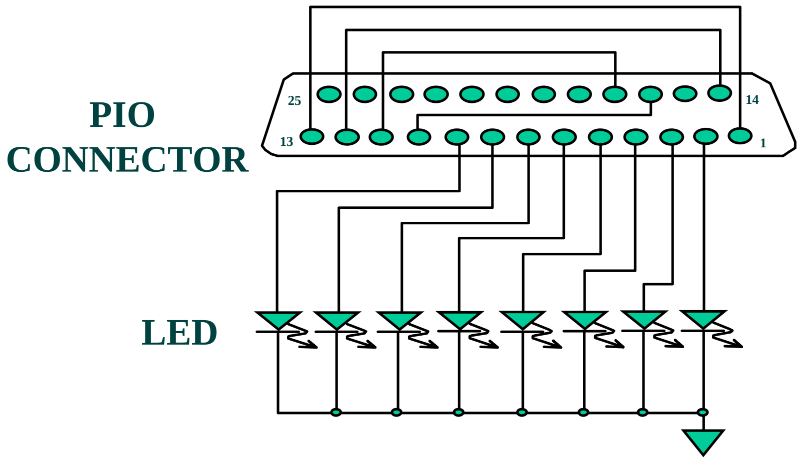
The 378 Port Debug Card, a kind of tool, is designed mainly for Notebook . It can be used to test the process of BIOS POST system. It composed of eight . LED and one PIO CONNECTOR as the below figure shows



P/N:411904800001
DESCRIPTION :PWA;PWA-378PORT DEBUG BD
Note:Order it from MIC/TSSC

7.3 Debug Card

7.3.2 CIRCUIT:



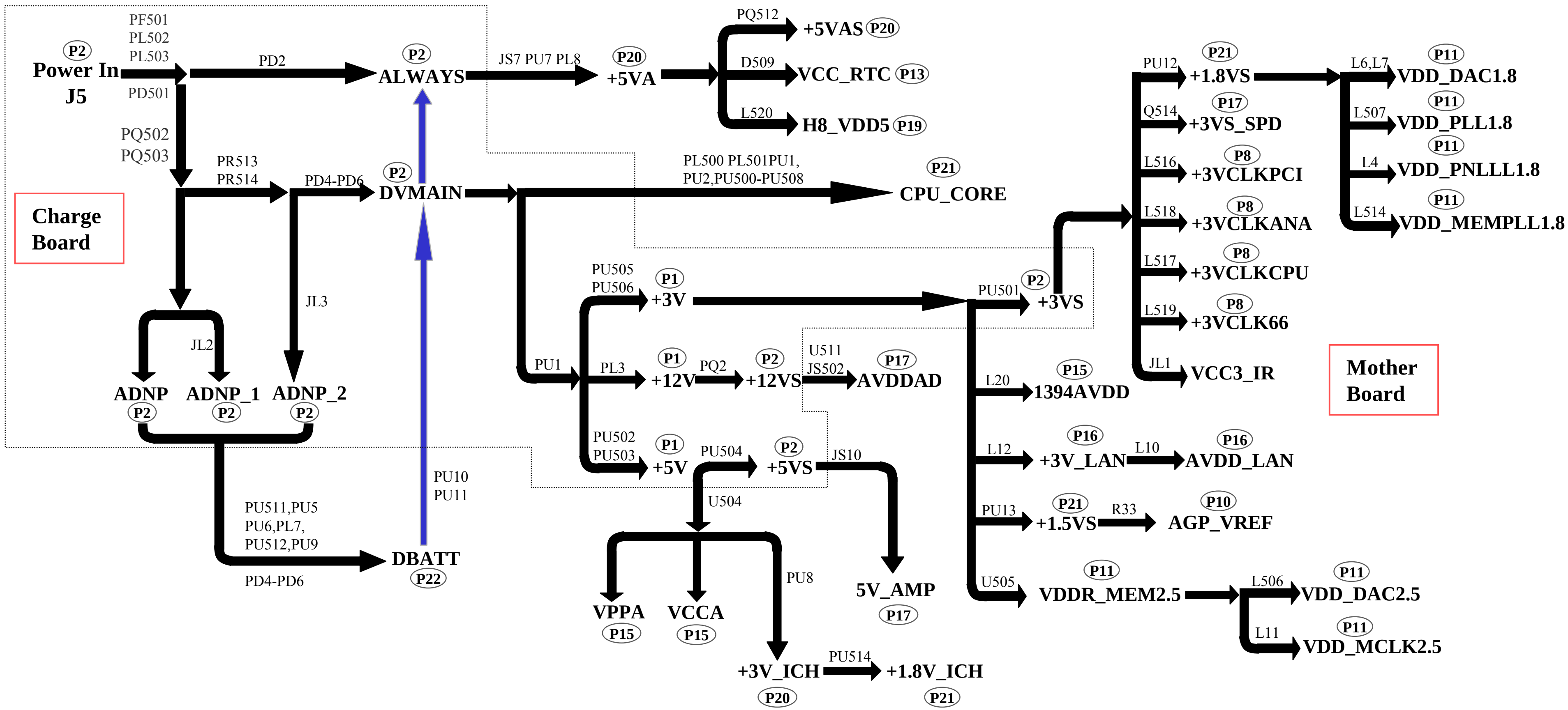
PIN DEFINITION OF PIO PORT					
PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN15	ERR	ERROR AT PRINTER
PIN10	ACK	ACKNOWLEDGE HANDSHANK	PIN16	INIT	INITIATE OUTPUT
PIN11	BUSY	BUSY SIGNAL	PIN17	SLIN	PRINTER SELECT
PIN12	PE	PAPER END	PIN18-25	SIGNAL GROUND	
PIN13	SLCT	PRINTER SELECTED			

8.Trouble Shooting

- 8.1 No Power
- 8.2 Battery Can not Be Charged
- 8.3 No Display
- 8.4 VGA Controller Failure LCD No Display
- 8.5 VGA Controller Failure External Monitor No Display
- 8.6 Memory Test Error
- 8.7 Keyboard(K/B) and Touch Pad(T/B) Test Error
- 8.8 Hard Drive Test Error
- 8.9 CD-ROM Drive Test Error
- 8.10 USB Port Test Error
- 8.11 PIO Port Test Error
- 8.12 PC-Card Failure
- 8.13 IEEE1394 Failure
- 8.14 Audio Failure
- 8.15 LAN Test Error

8.1 No Power

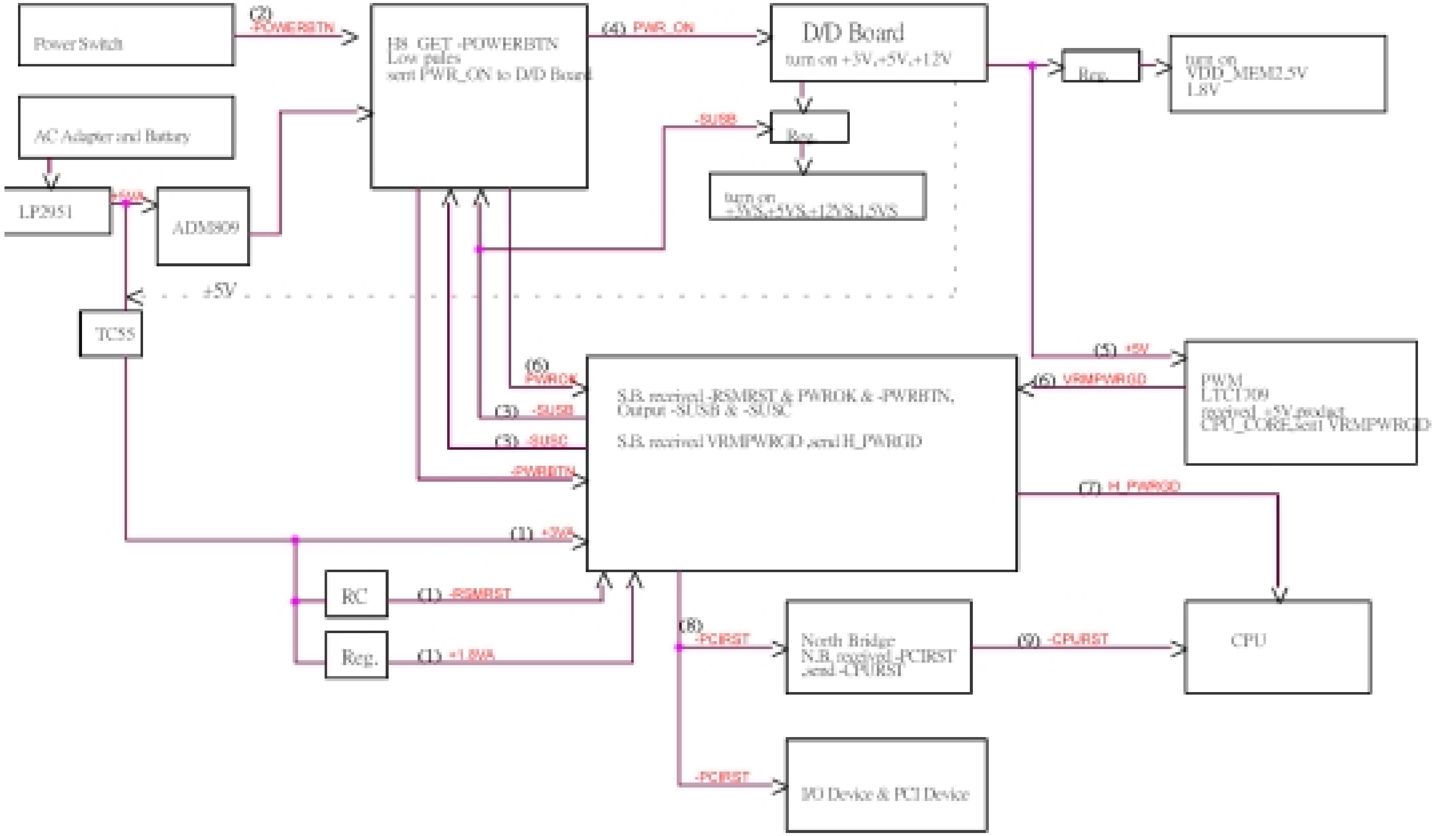
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power (1)

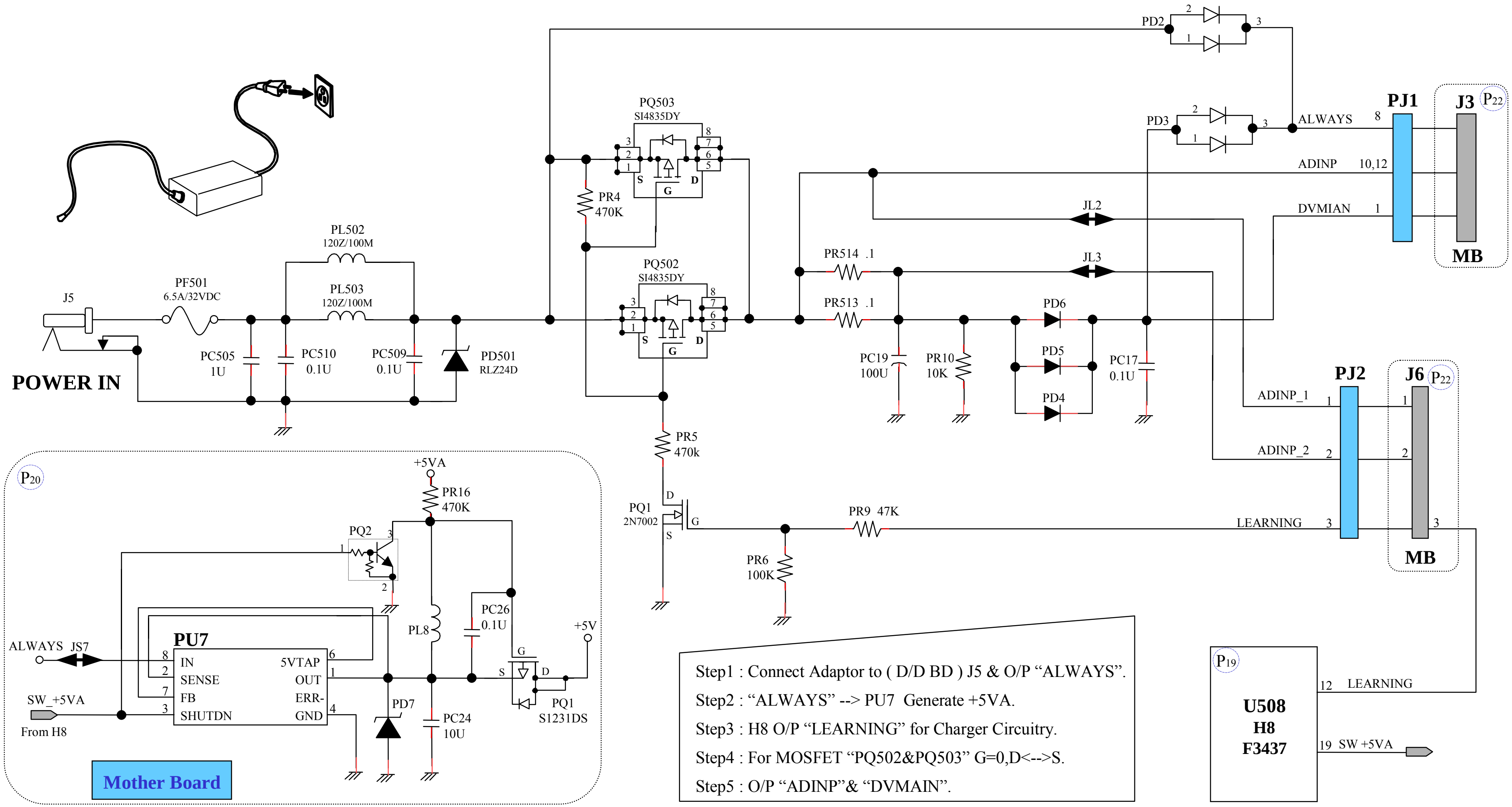
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Power on Sequence



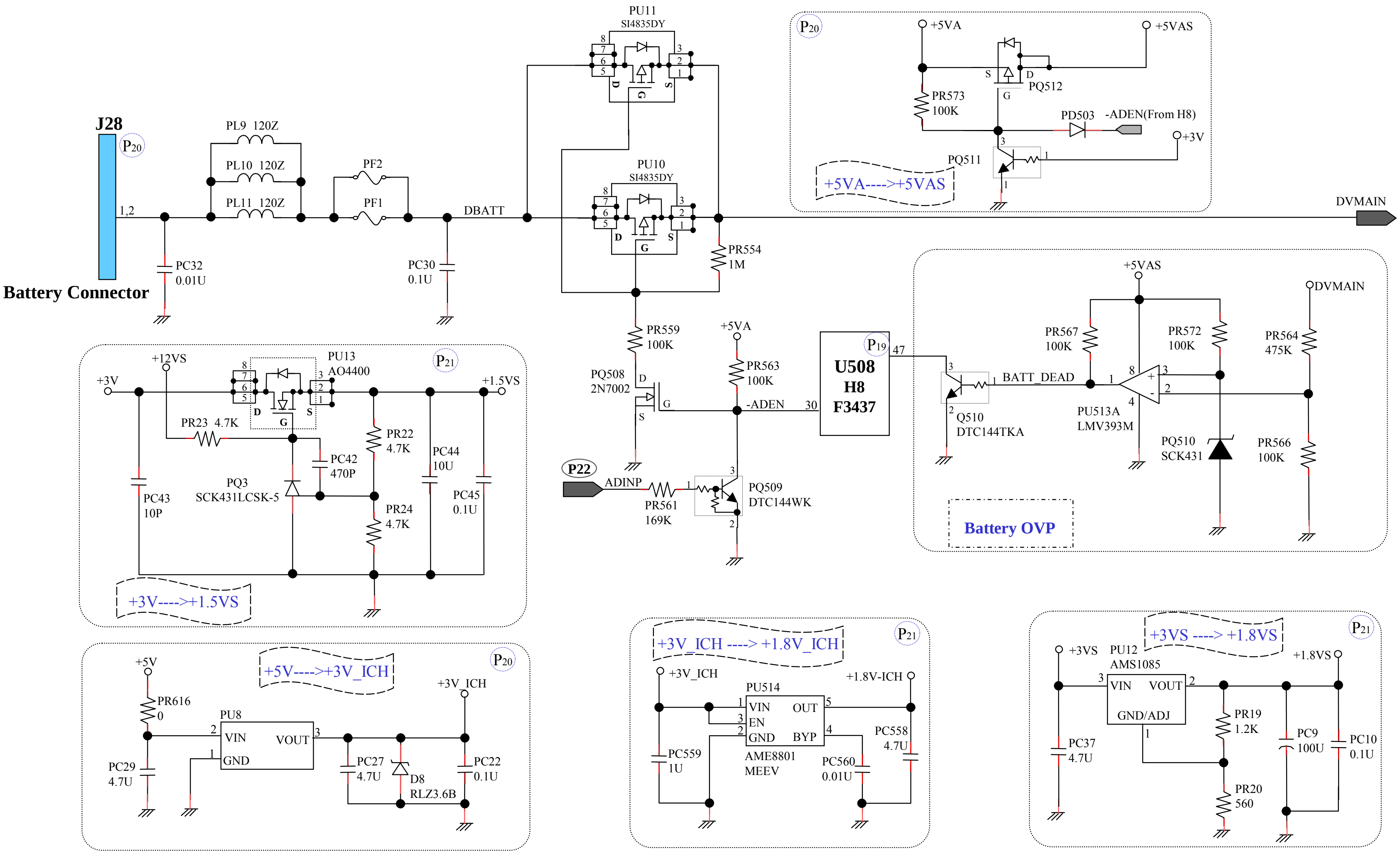
8.1 No Power (2)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



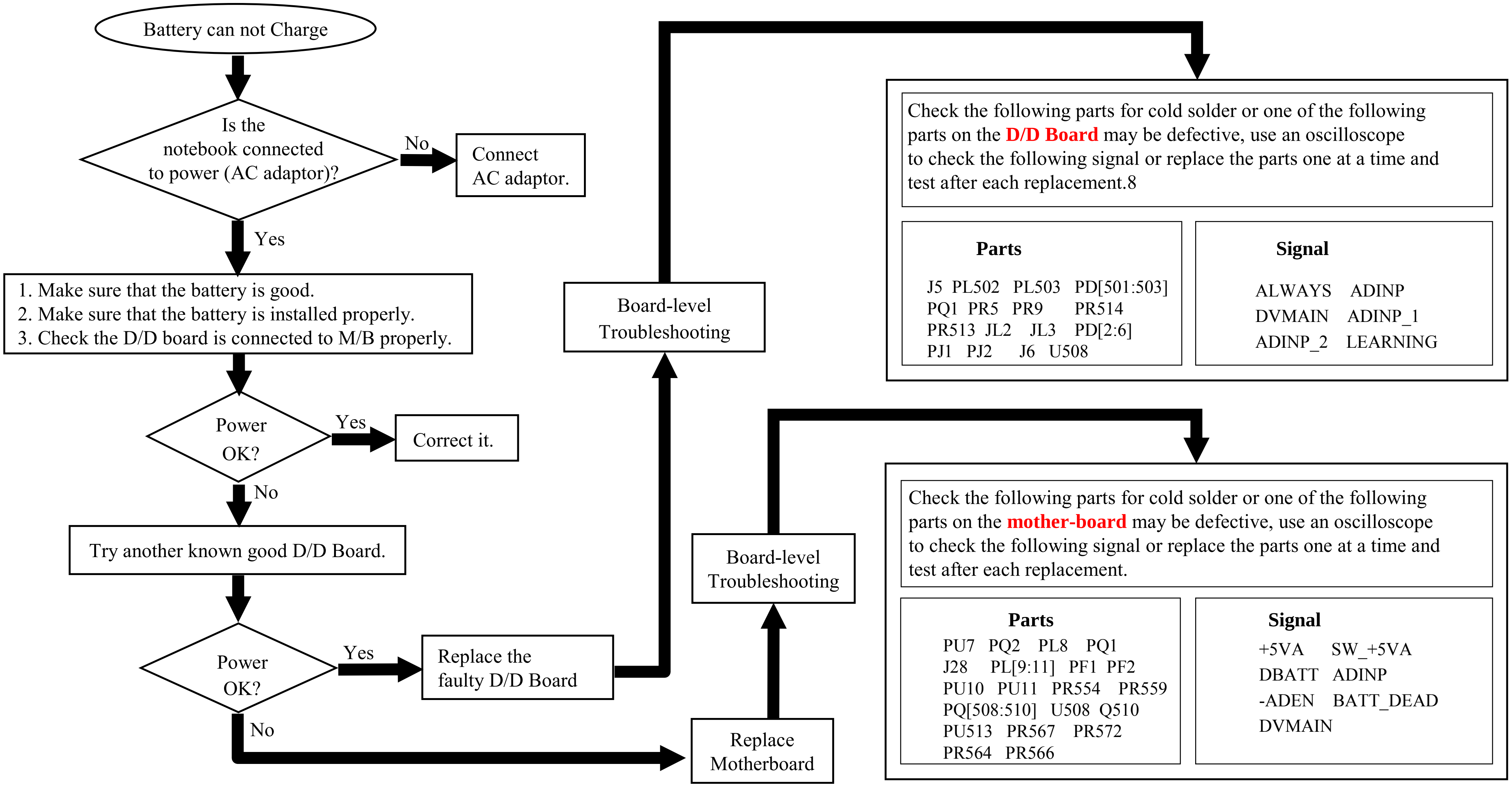
8.1 No Power (3)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



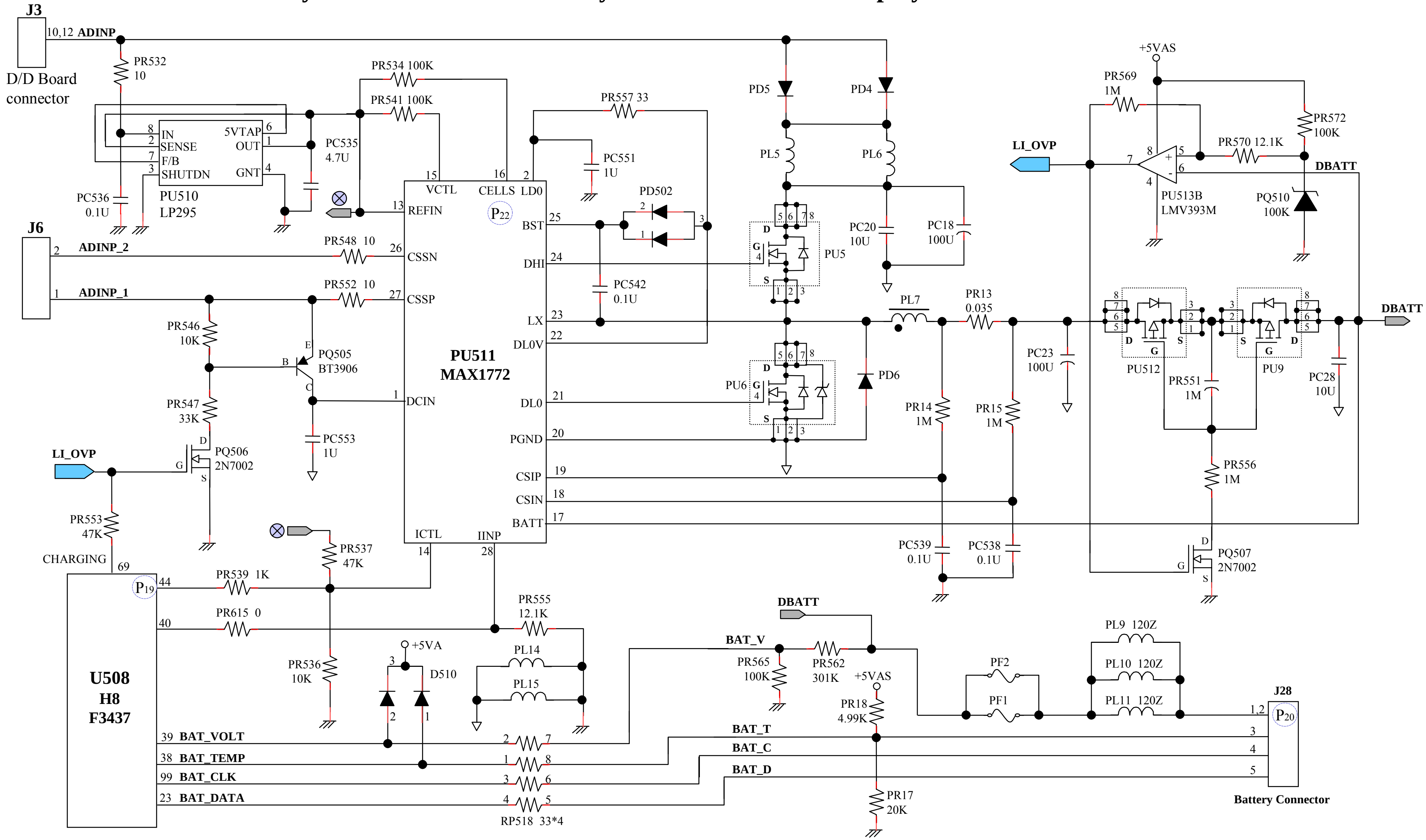
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



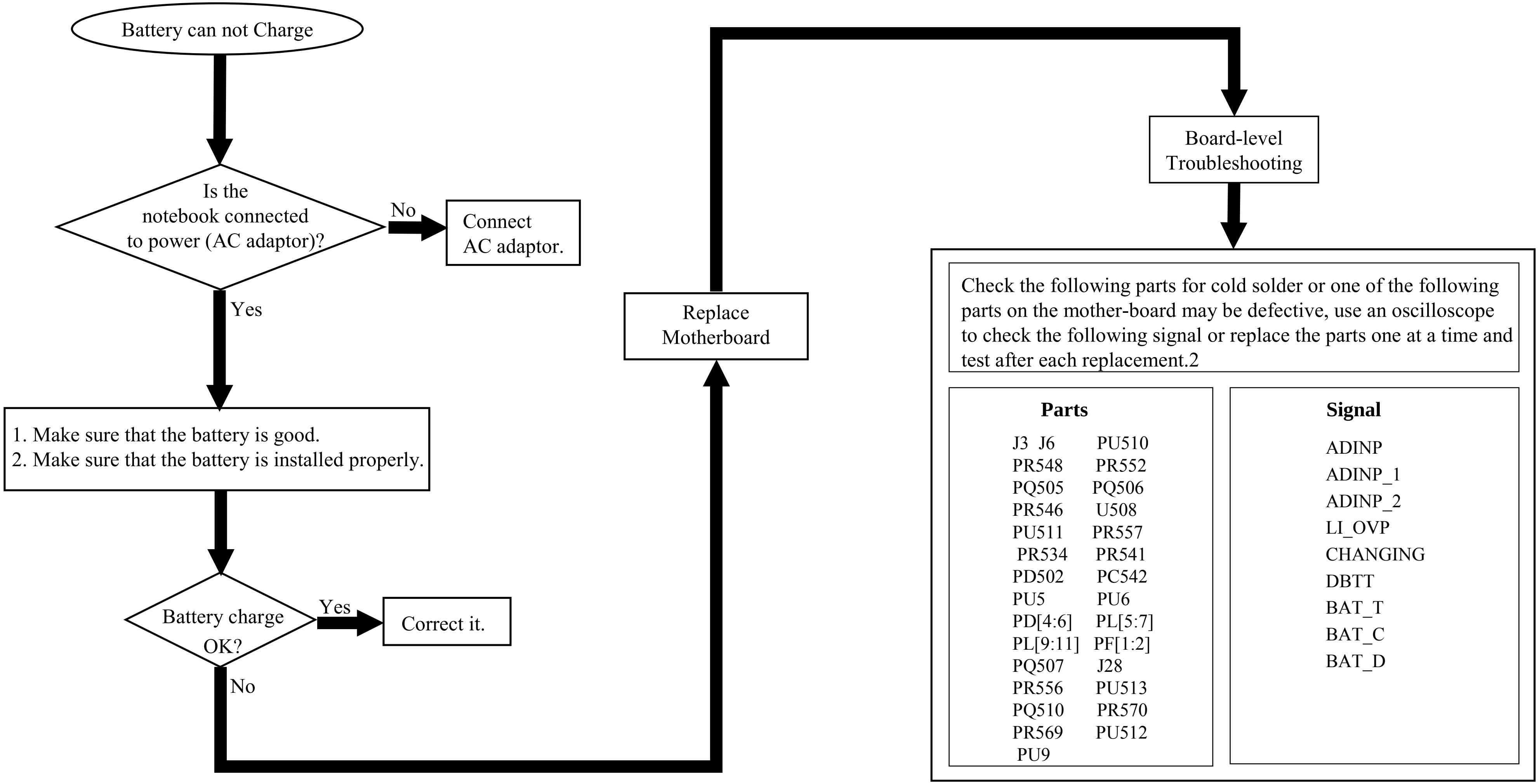
8.2 Battery Can not Be Change

When the battery is installed but the battery status indicate LED display abnormal.



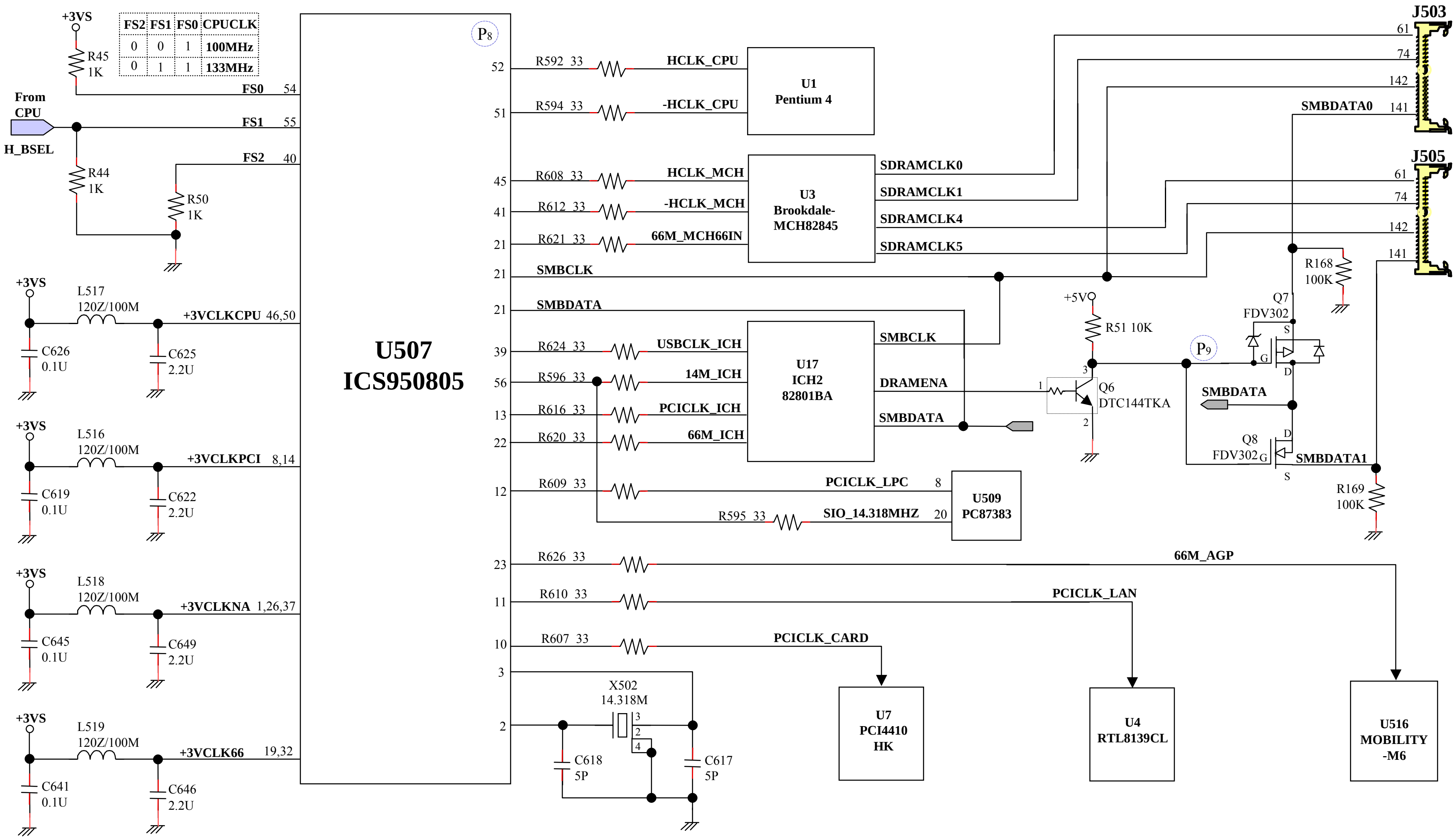
8.2 Battery Can not Be Change

When the battery is installed but the battery status indicate LED display abnormal.

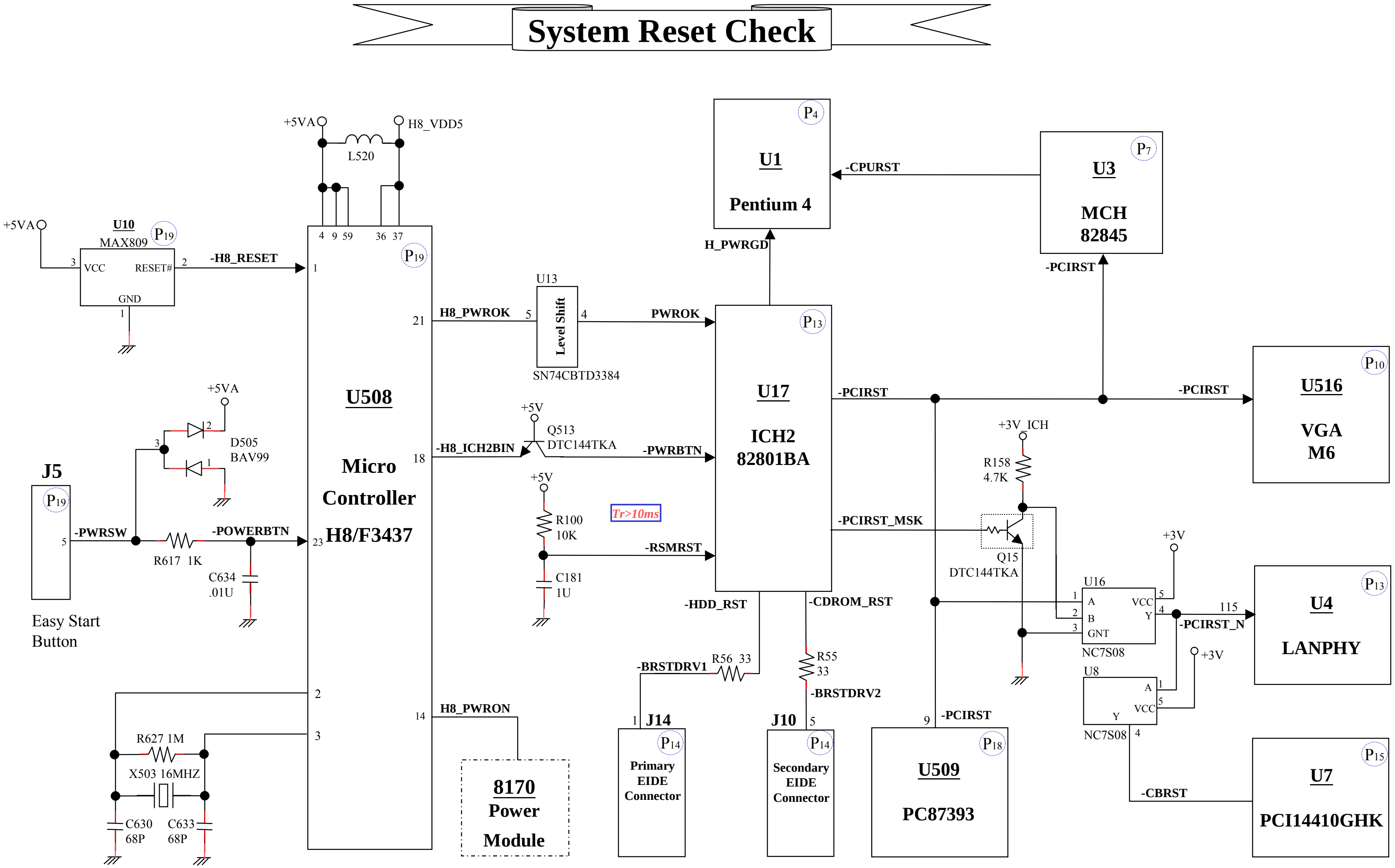


8.3 No Display

System Clock Check

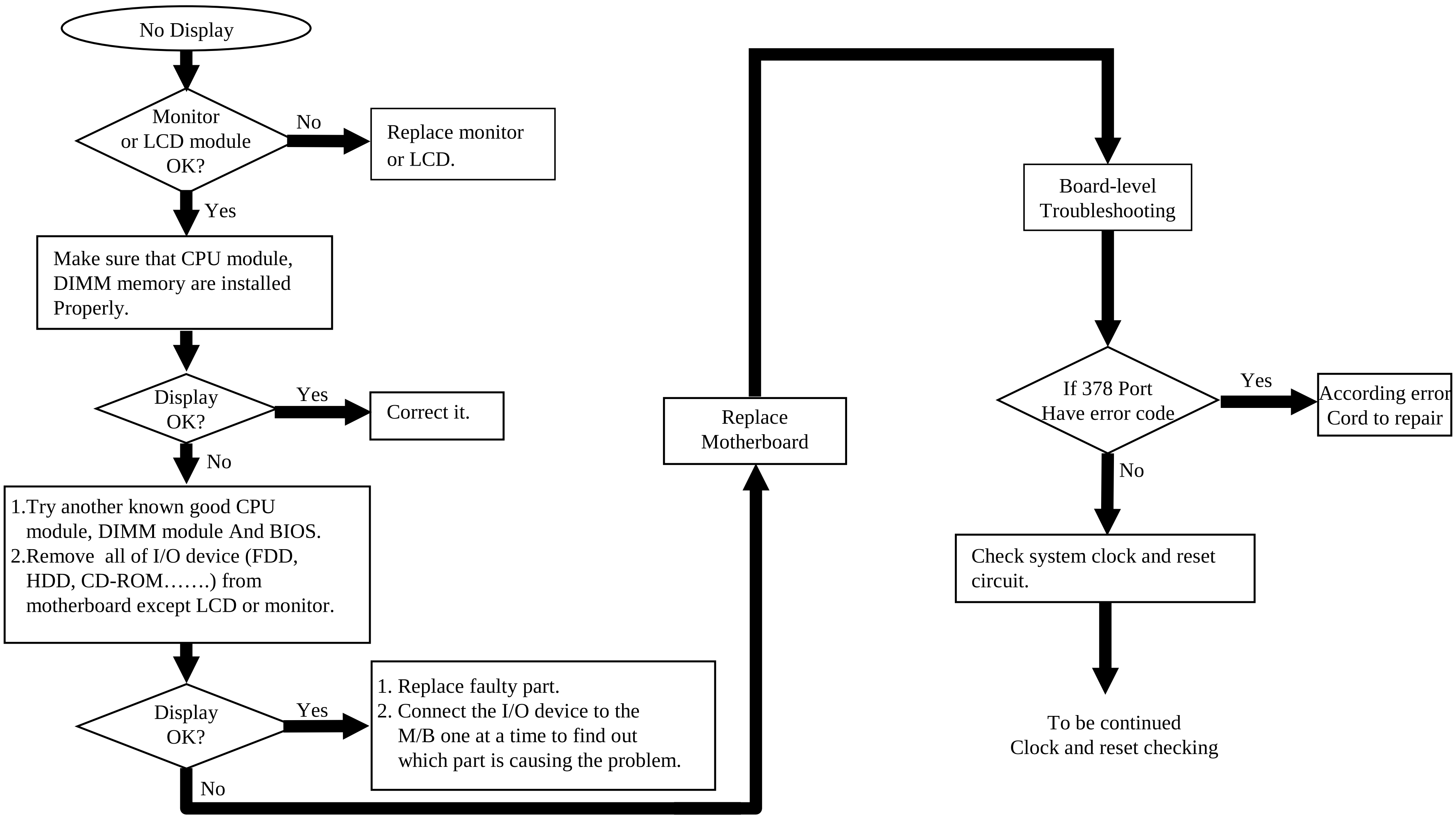


8.3 No Display



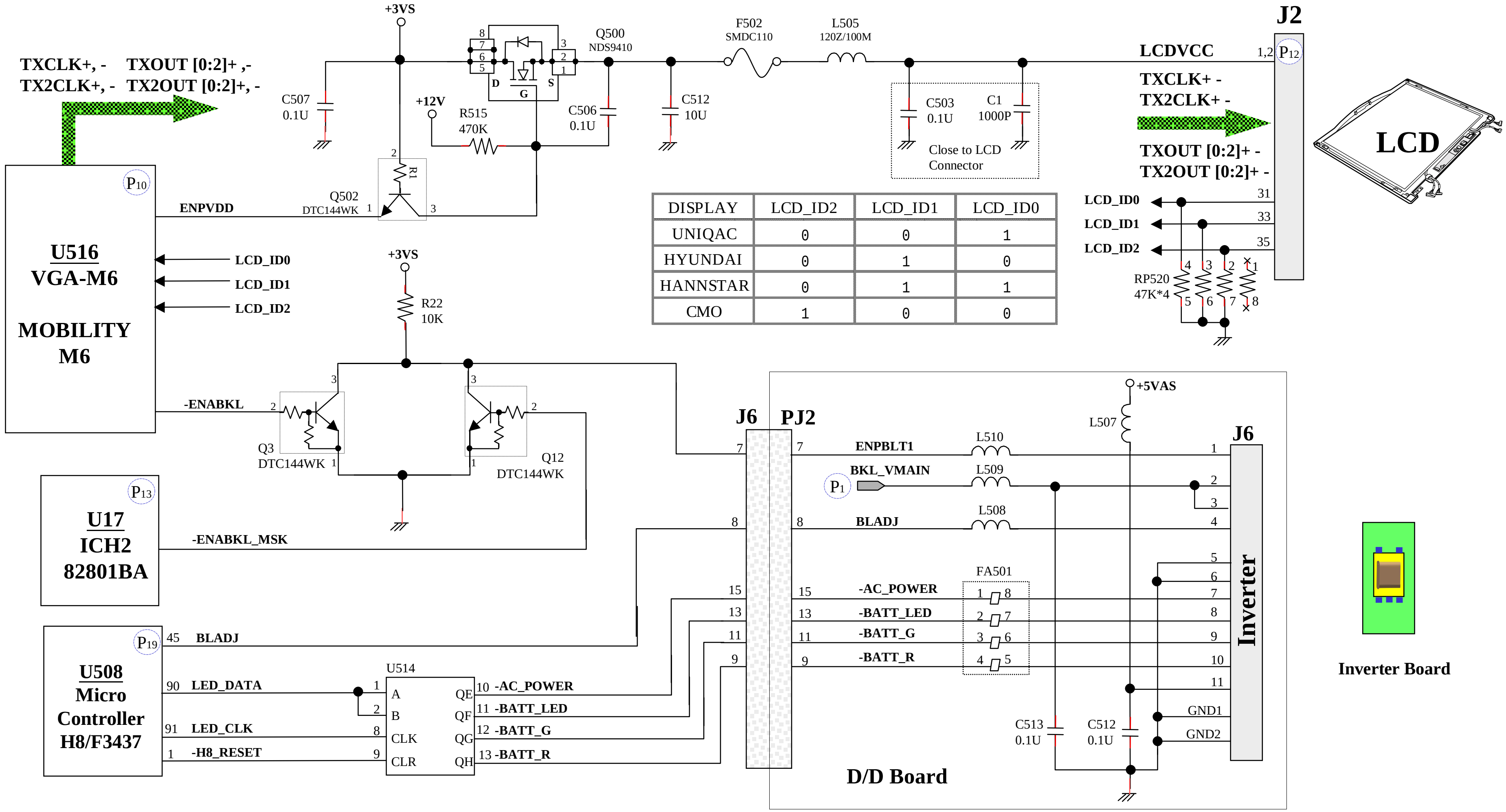
8.3 No Display

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



8.4 VGA Controller Failure LCD No Display

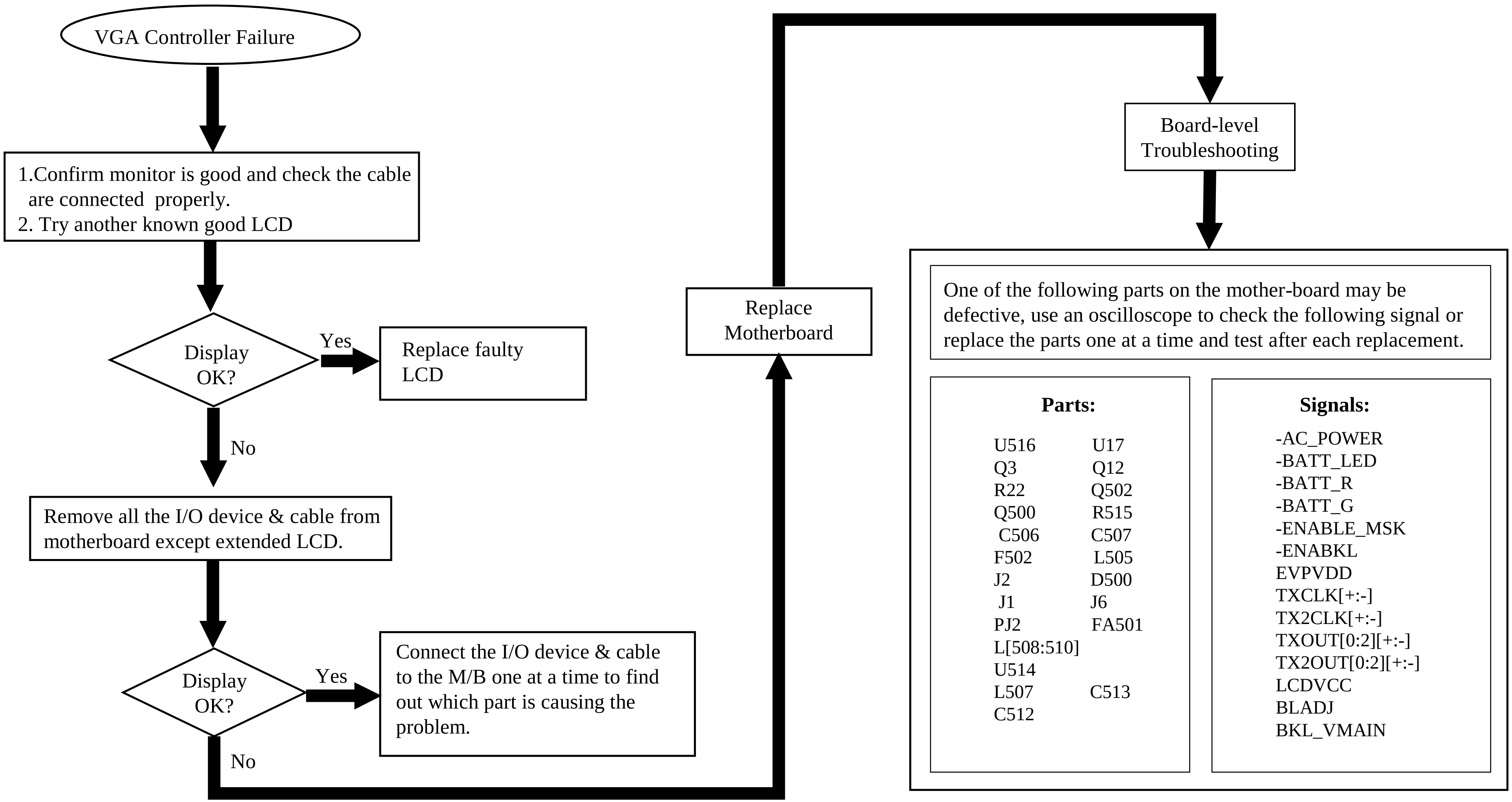
There is no display or picture abnormal on LCD or monitor.



DISPLAY	LCD_ID2	LCD_ID1	LCD_ID0
UNIQAC	0	0	1
HYUNDAI	0	1	0
HANNSTAR	0	1	1
CMO	1	0	0

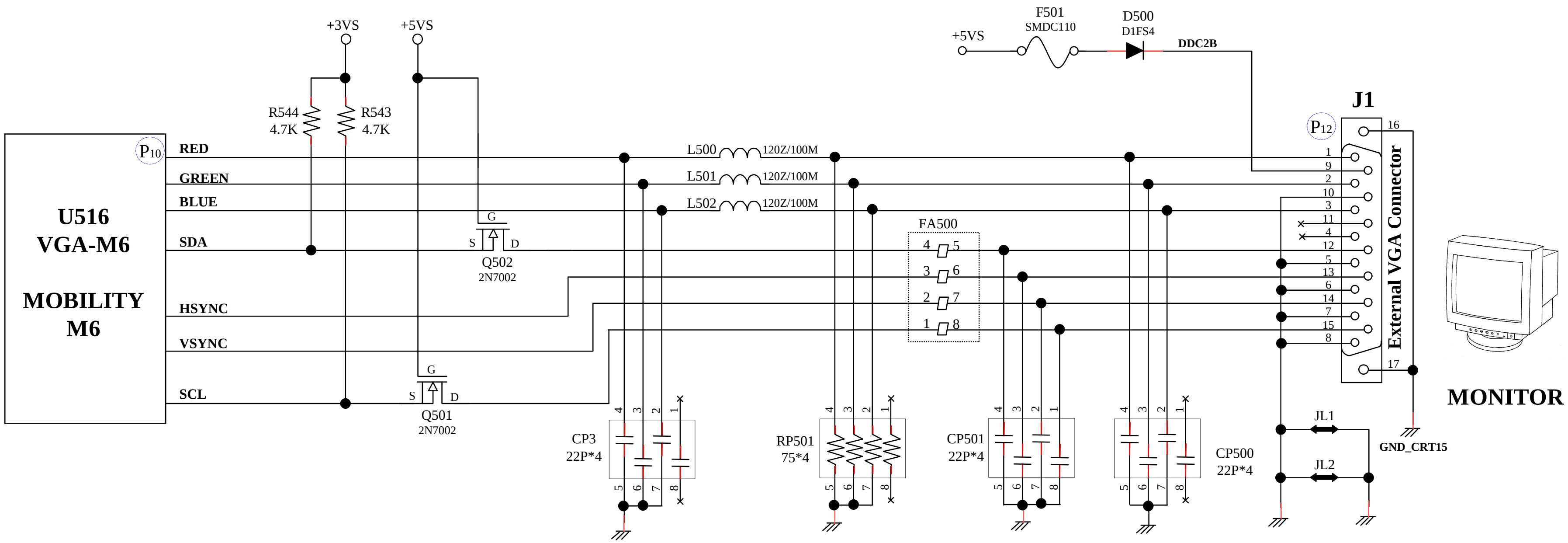
8.4 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD or monitor.



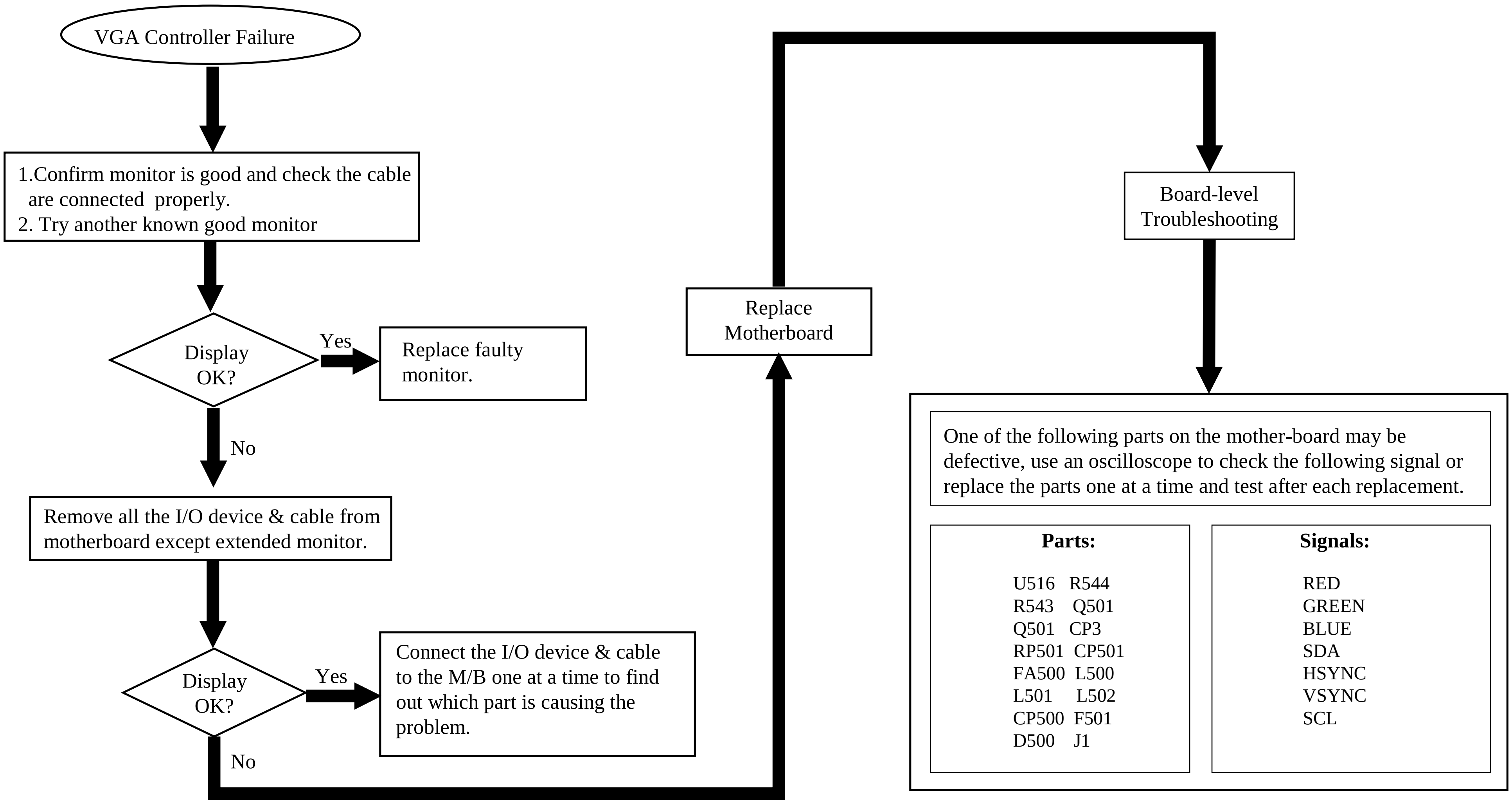
8.5 VGA Controller Failure Monitor No Display

There is no display or picture abnormal on monitor.



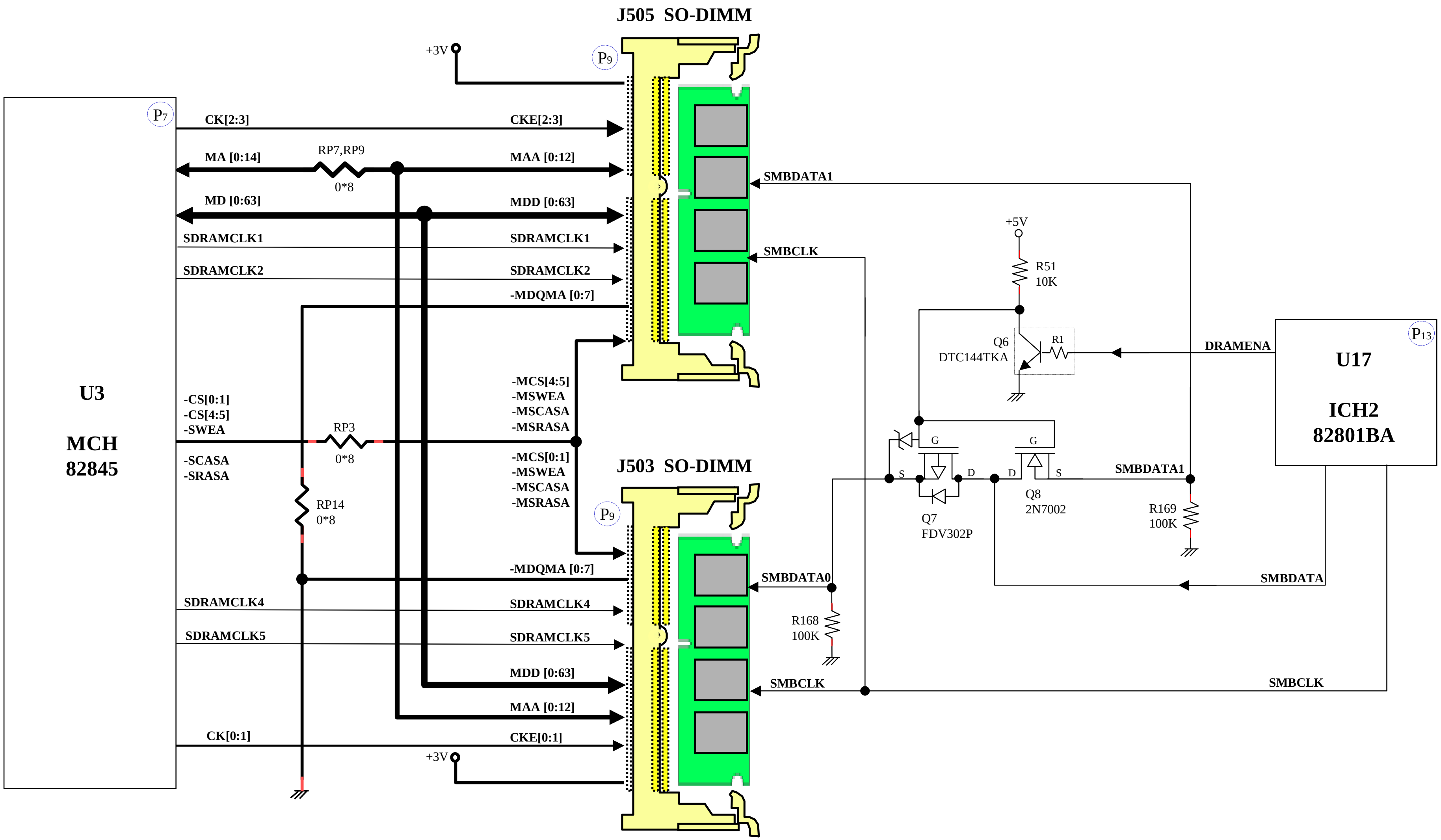
8.5 VGA Controller Failure Monitor No Display

There is no display or picture abnormal on monitor.



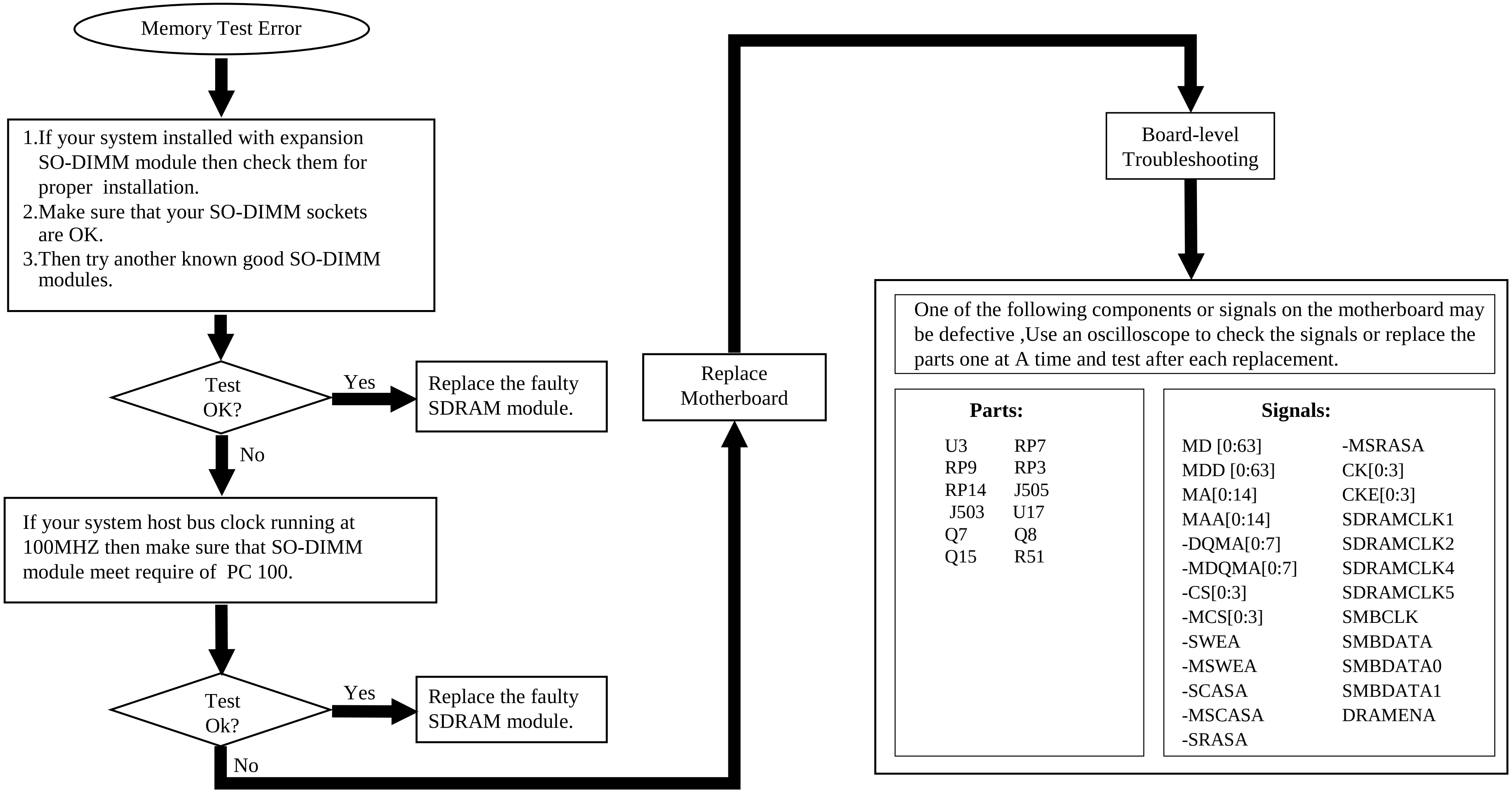
8.6 Memory Test Error

Either one or two extend SO-DIMM RAM Module is failure or system hangs up.



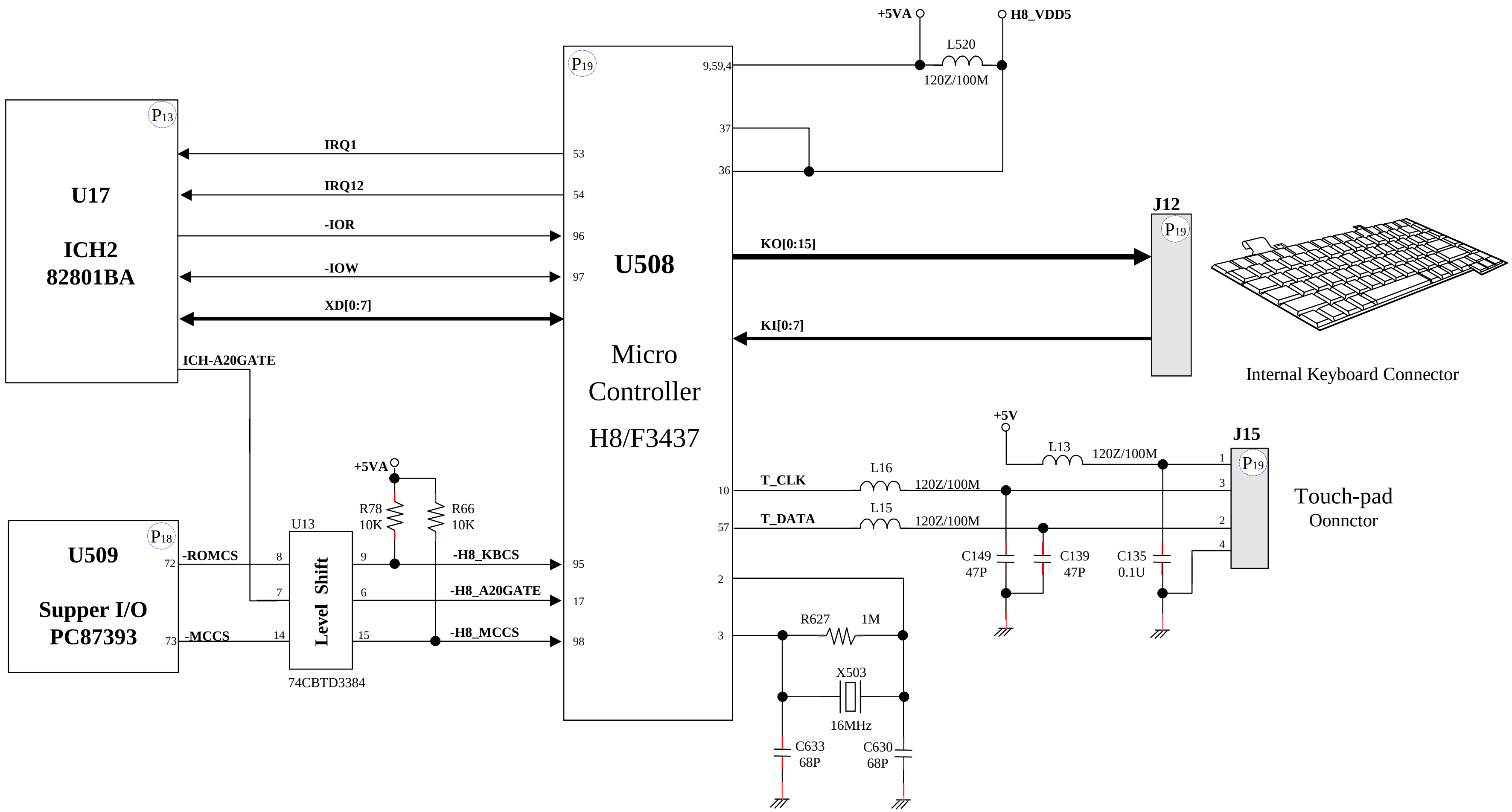
8.6 Memory Test Error

Either one or two extend SO-DIMM RAM Module is failure or system hangs up.



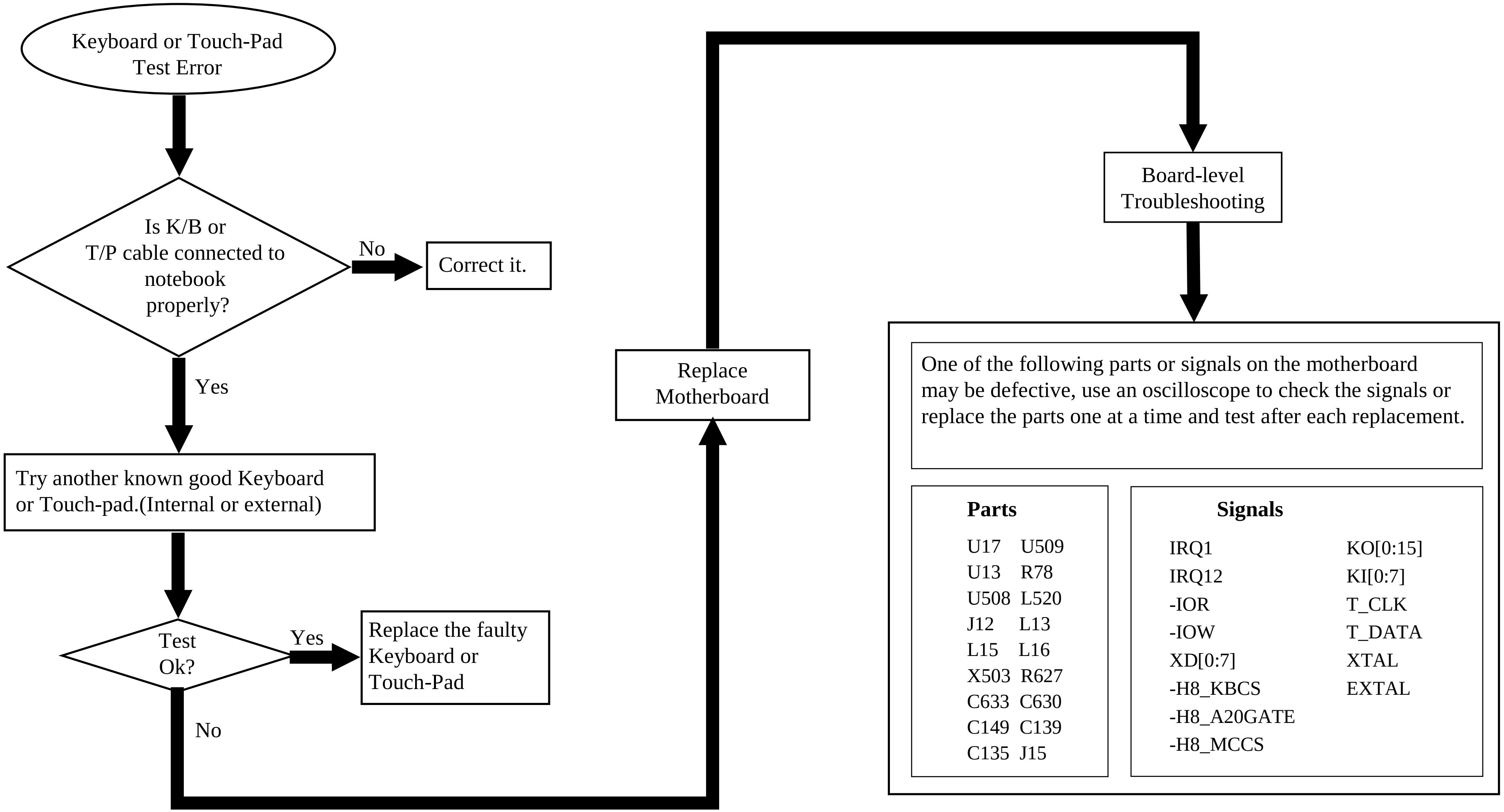
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



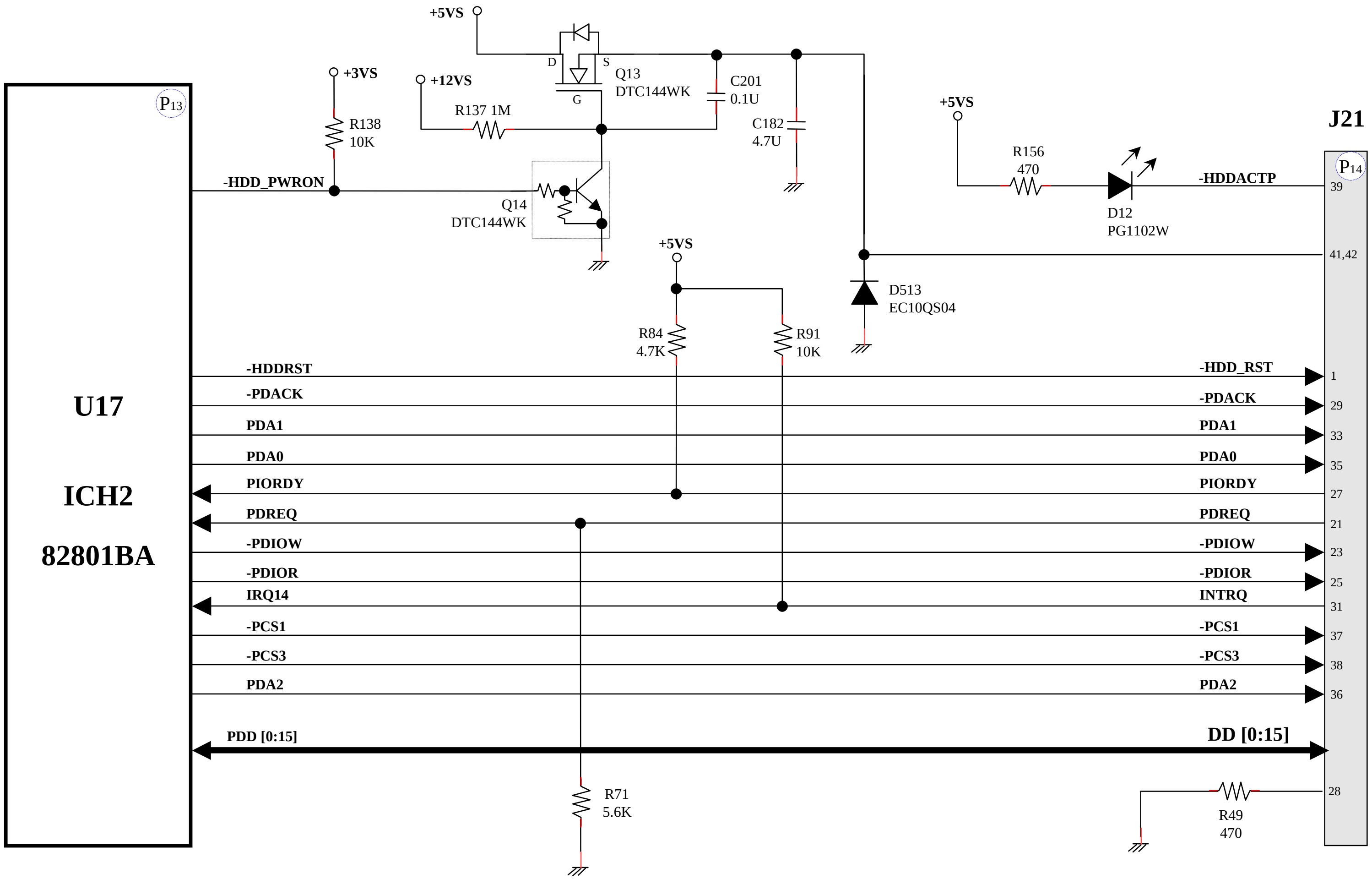
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

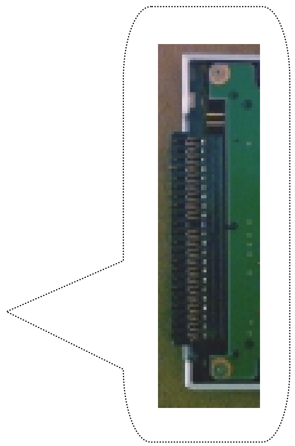
Error message of keyboard or touch-pad failure is shown or any key does not work.



8.8 Hard Drive Test Error

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



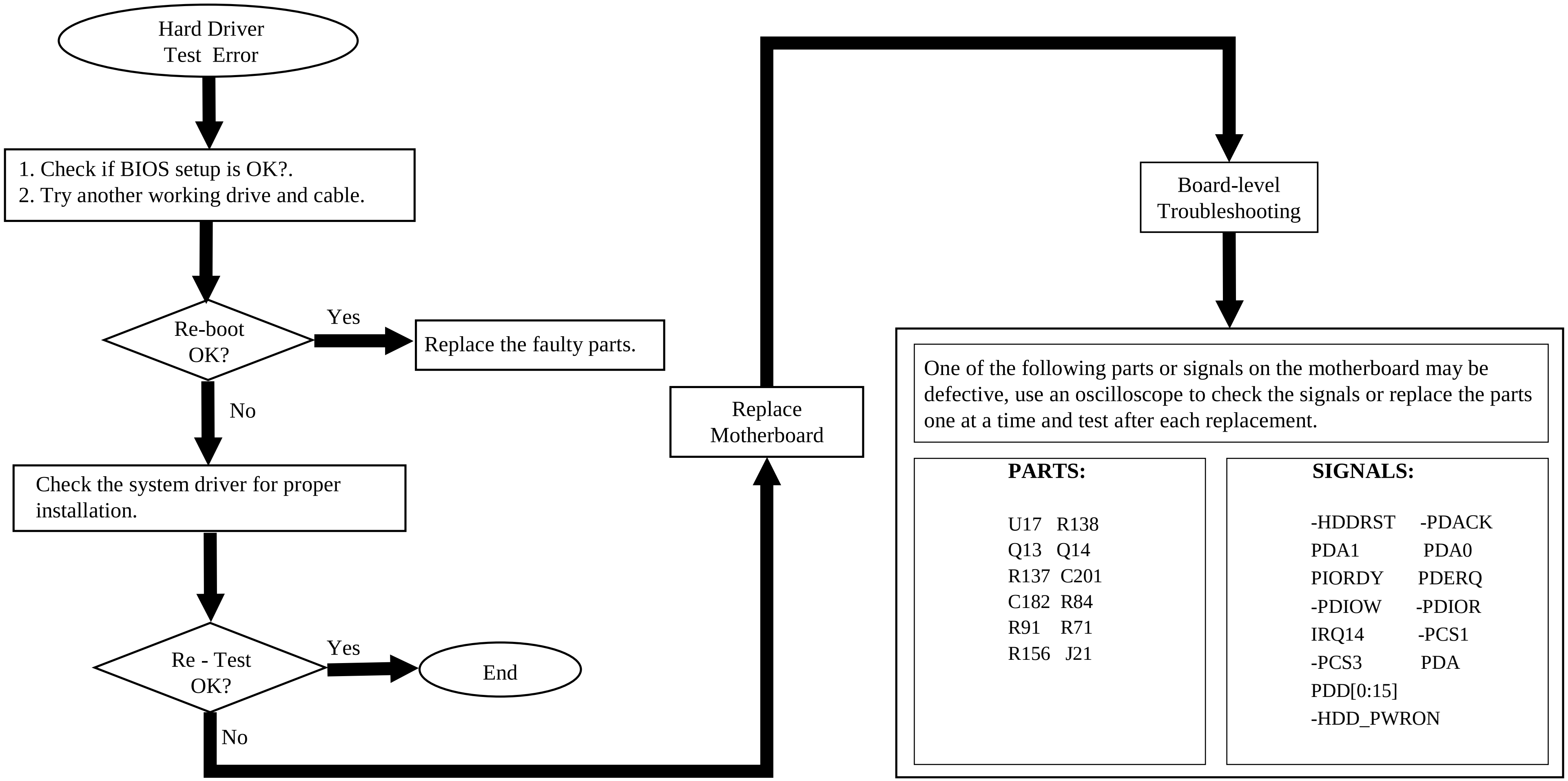




Primary EIDE Connector
For Hard Disk

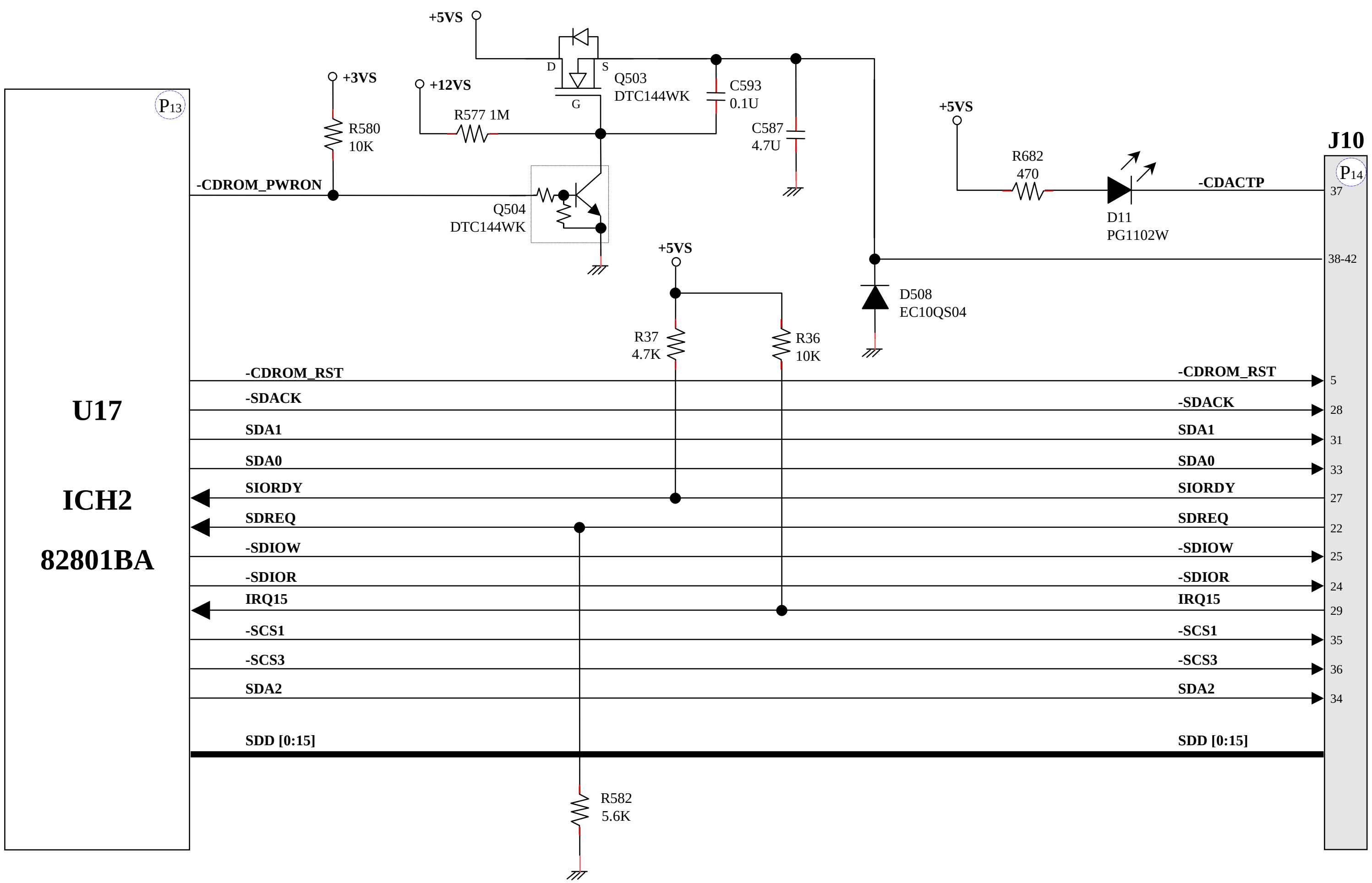
8.8 Hard Drive Test Error

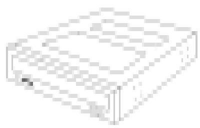
Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



8.9 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.

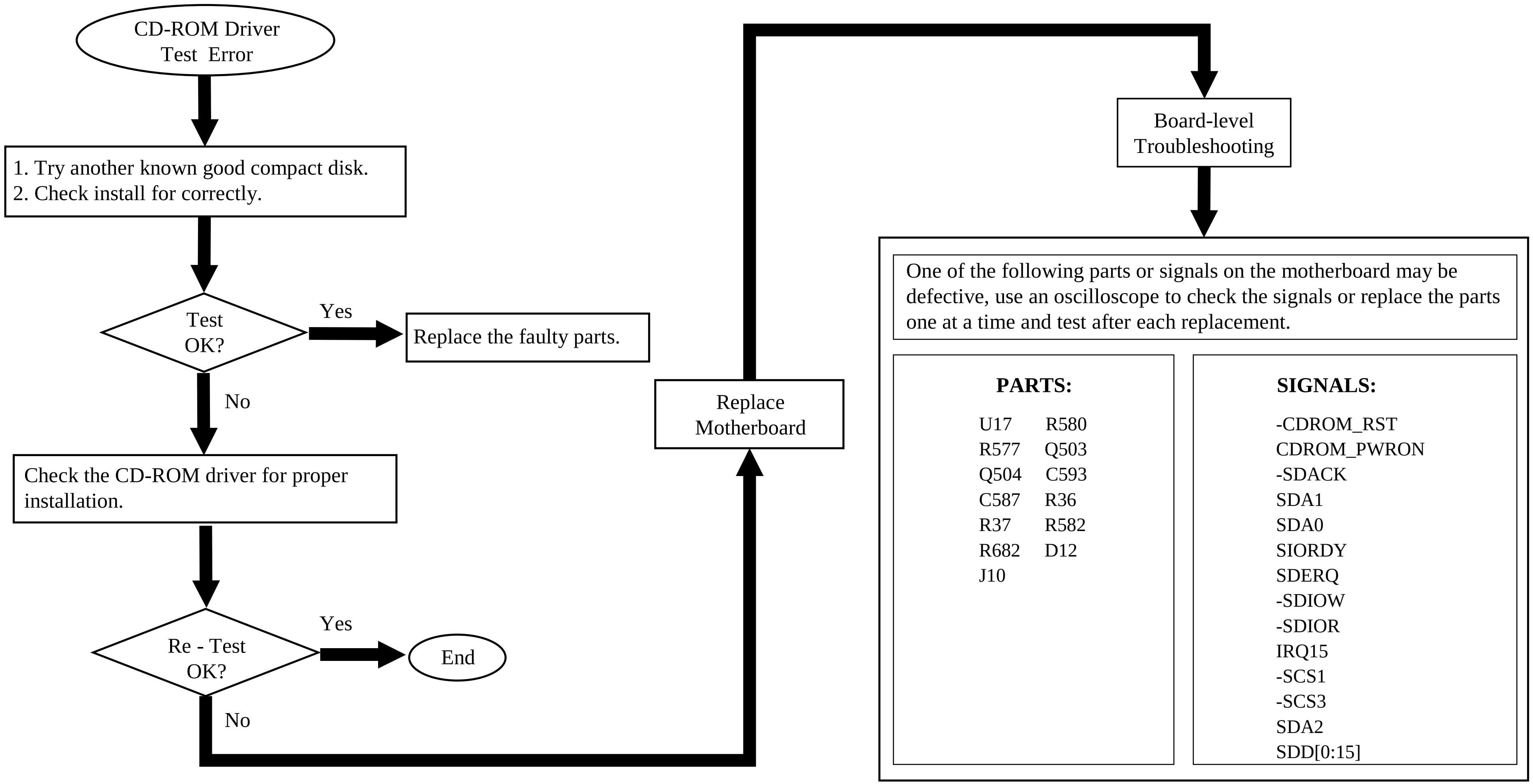




Secondary EIDE Connector
For CD-ROM

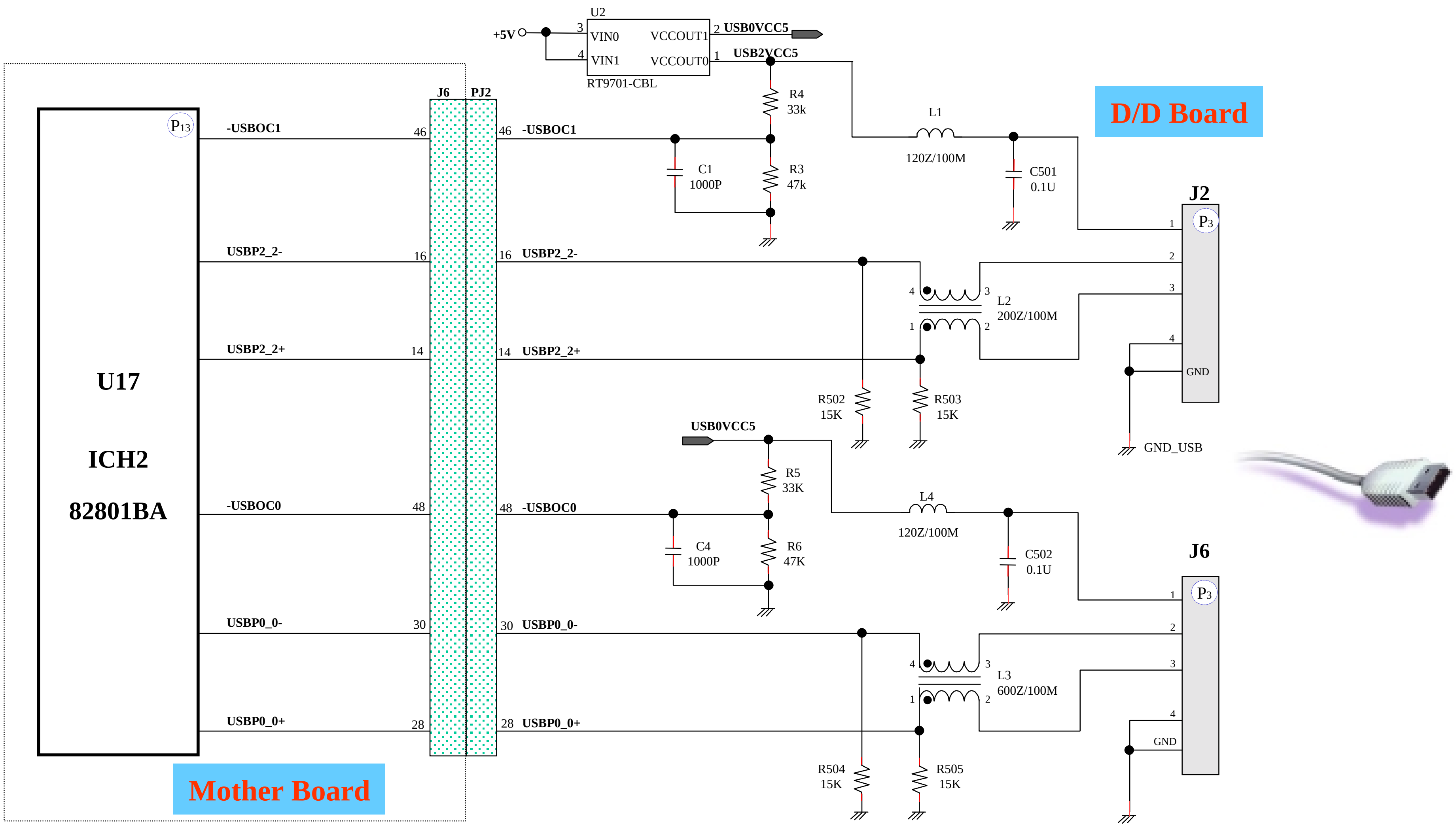
8.9 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



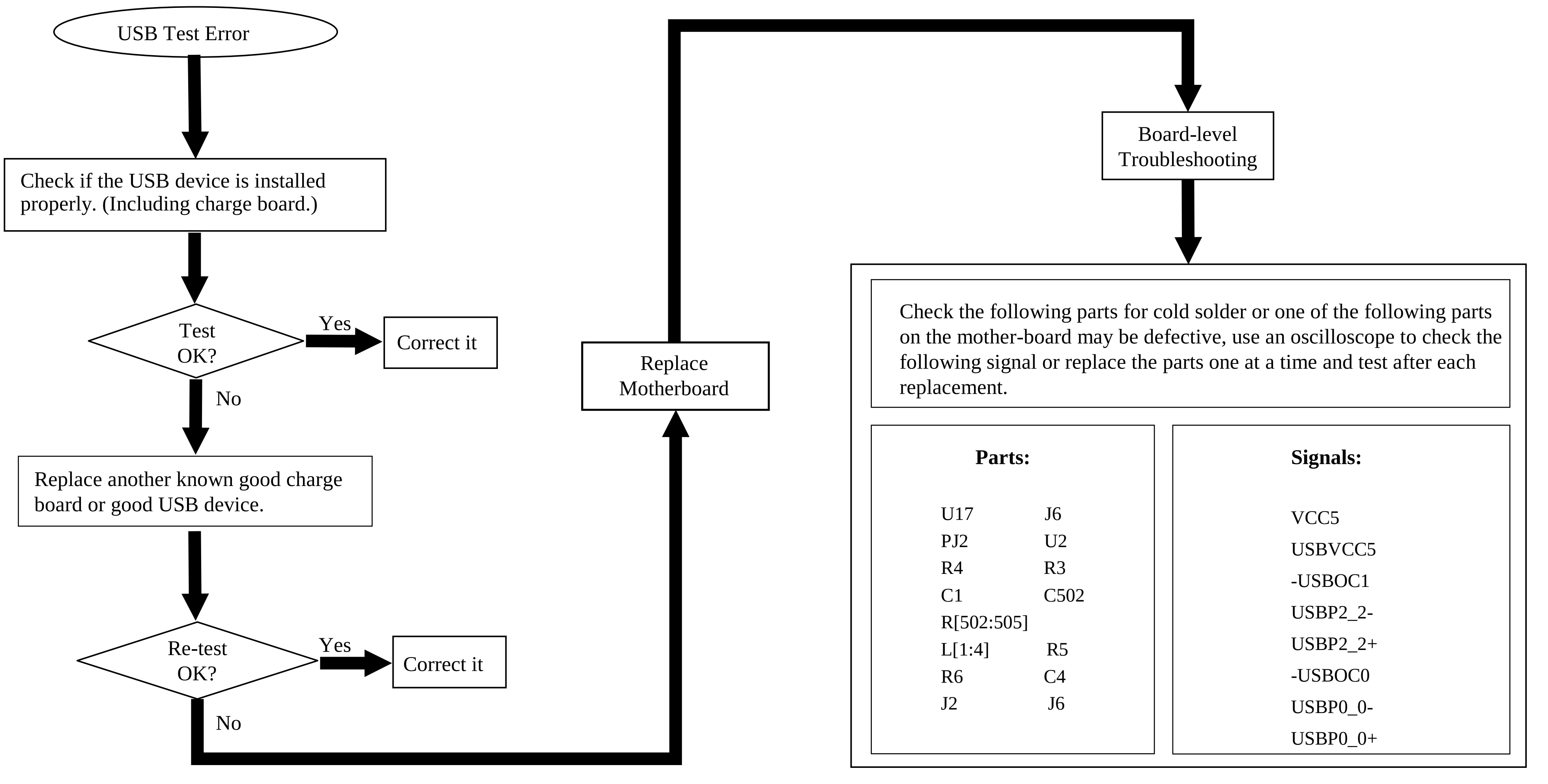
8.10 USB Port Test Error

An error occurs when a USB I/O device is installed.



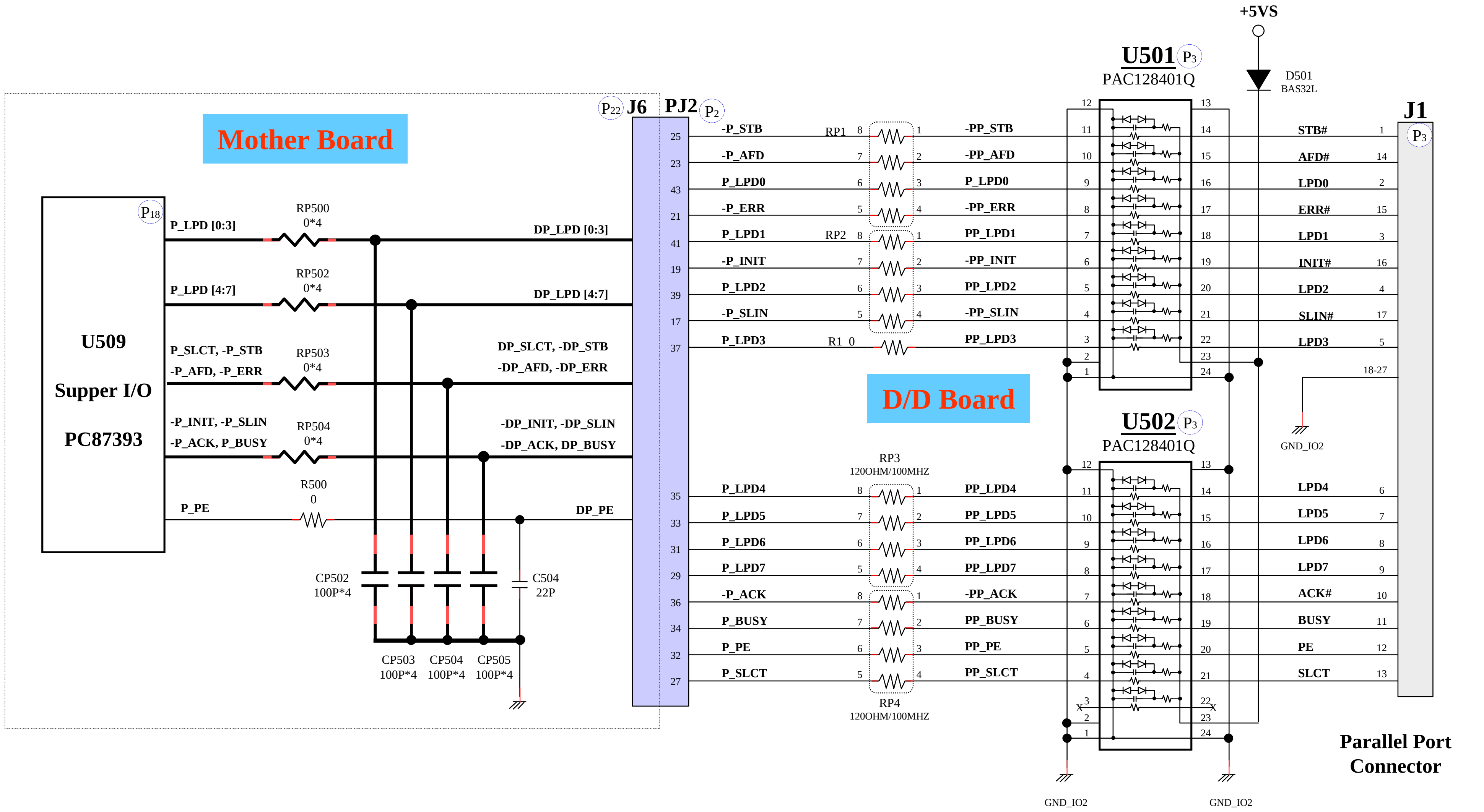
8.10 USB Port Test Error

An error occurs when a USB I/O device is installed.



8.11 PIO Port Test Error

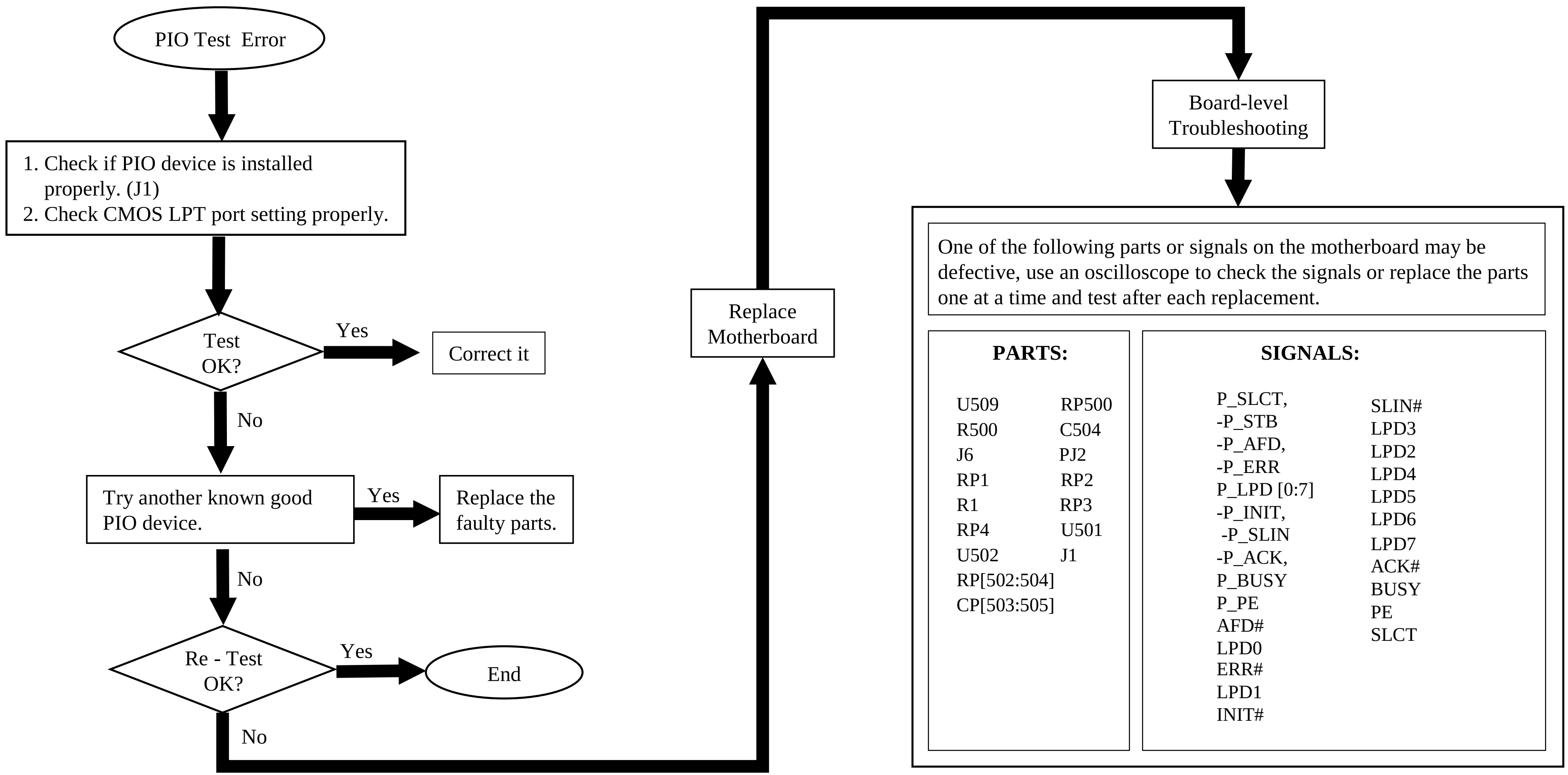
When a print command is issued, printer prints nothing or garbage.



Parallel Port Connector

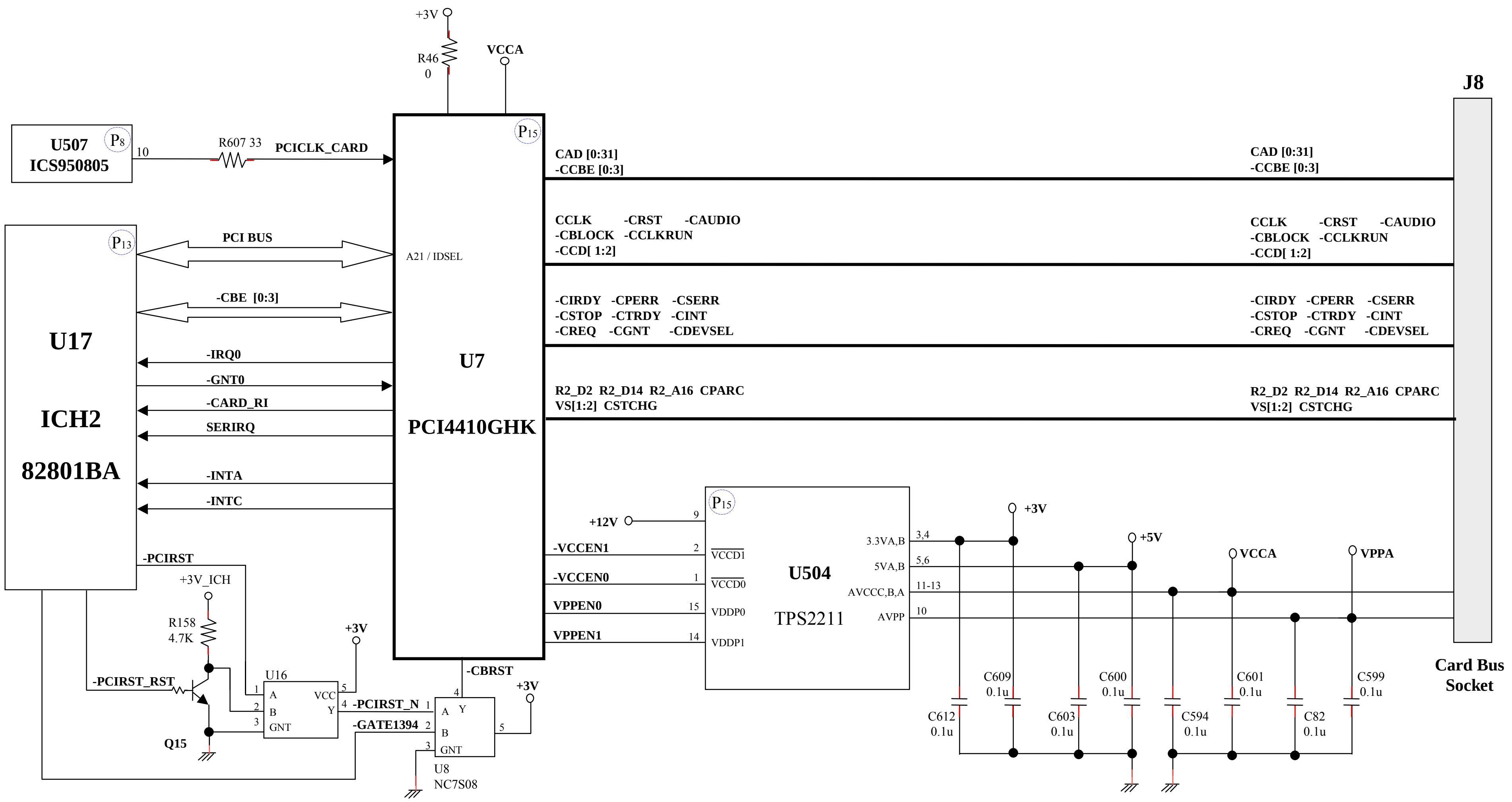
8.11 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



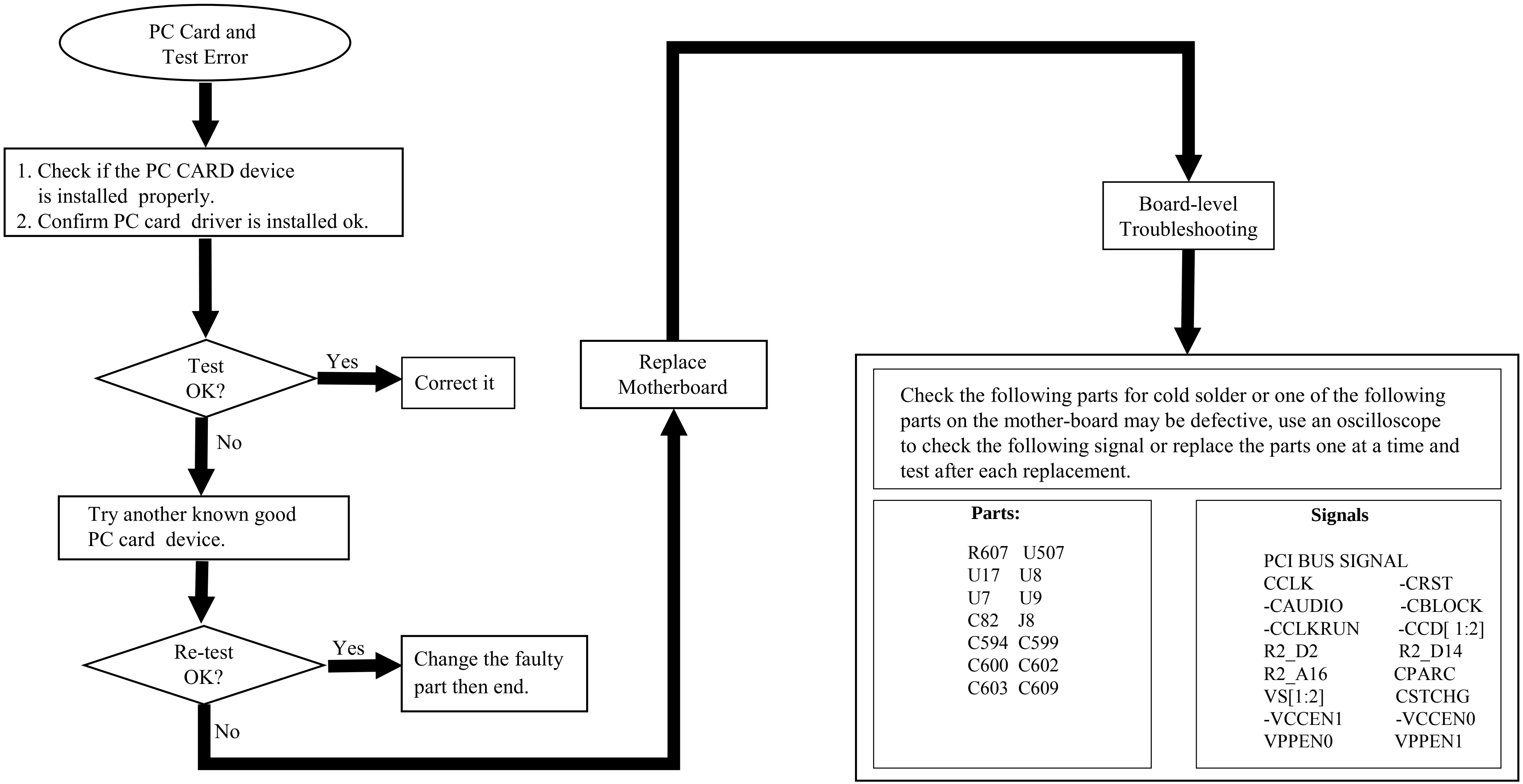
8.12 PC-Card Socket Failure

An error occurs when a PC card device is installed.



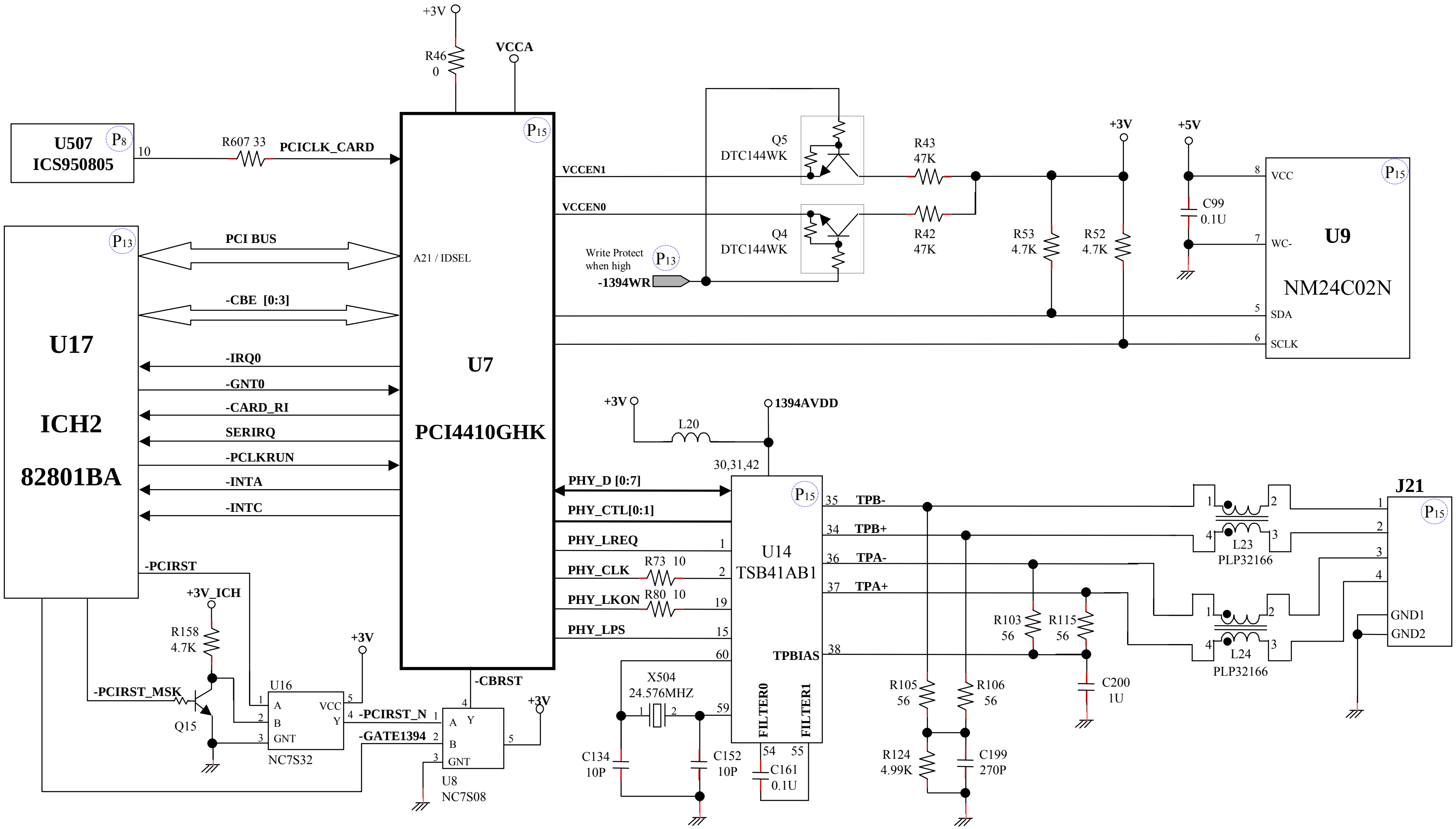
8.12 PC-Card Socket Failure

An error occurs when a PC card device is installed.



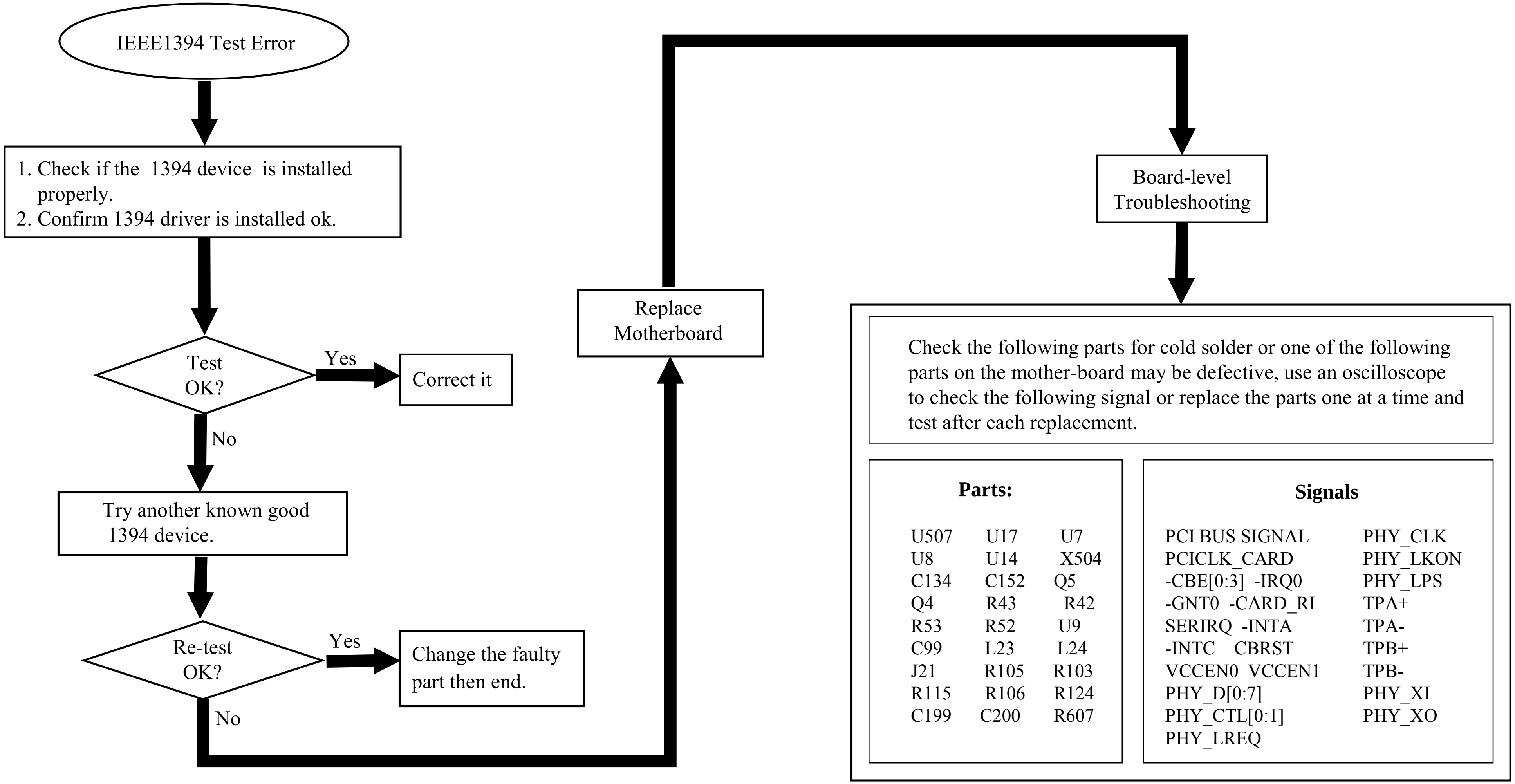
8.13 IEEE1394 Failure

An error occurs when a PC card device or 1394 device is installed.



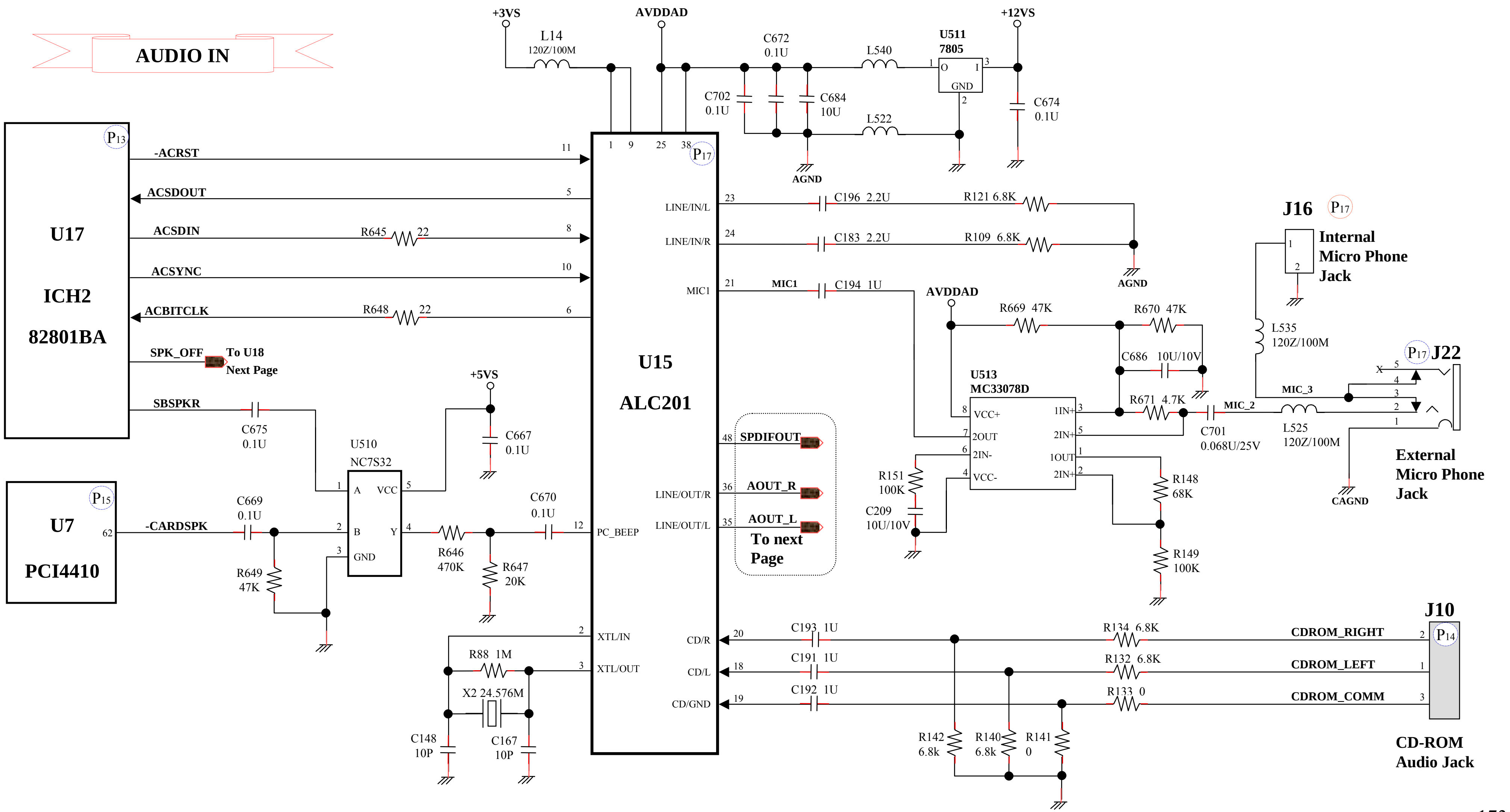
8.13 IEEE1394 Failure

An error occurs when a PC card device or 1394 device is installed.



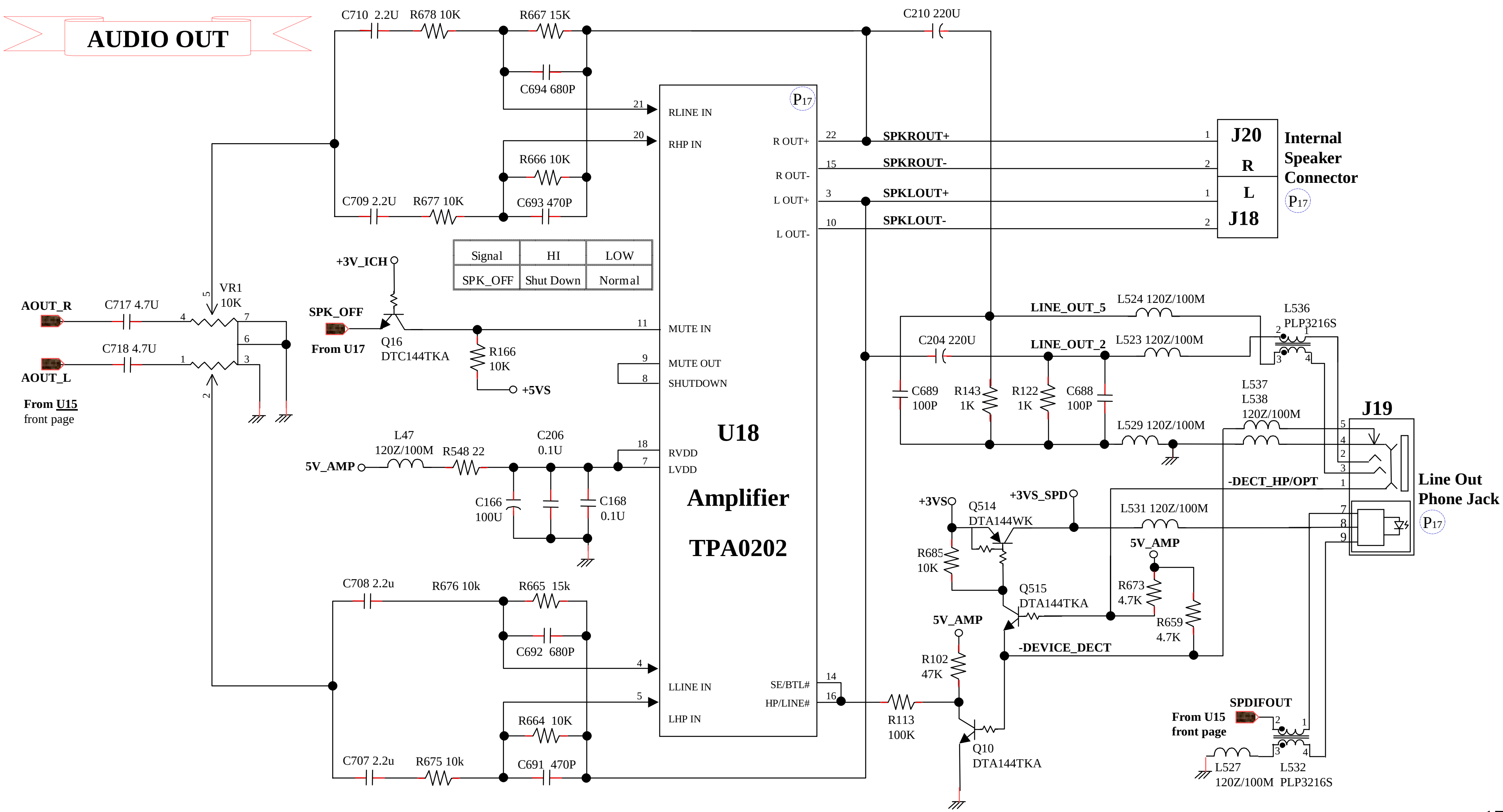
8.14 Audio Failure

No sound from speaker after audio driver is installed.



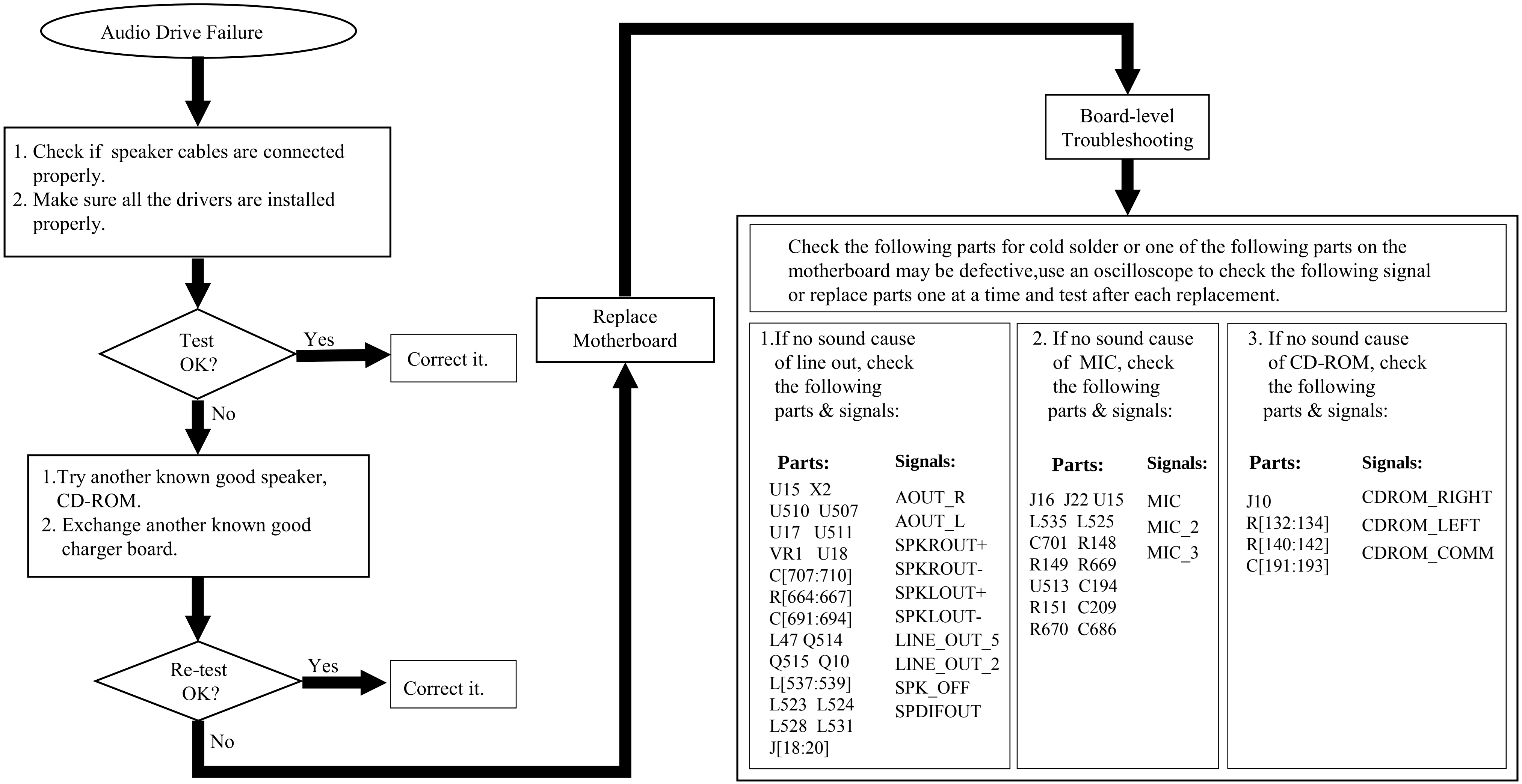
8.14 Audio Failure

No sound from speaker after audio driver is installed.



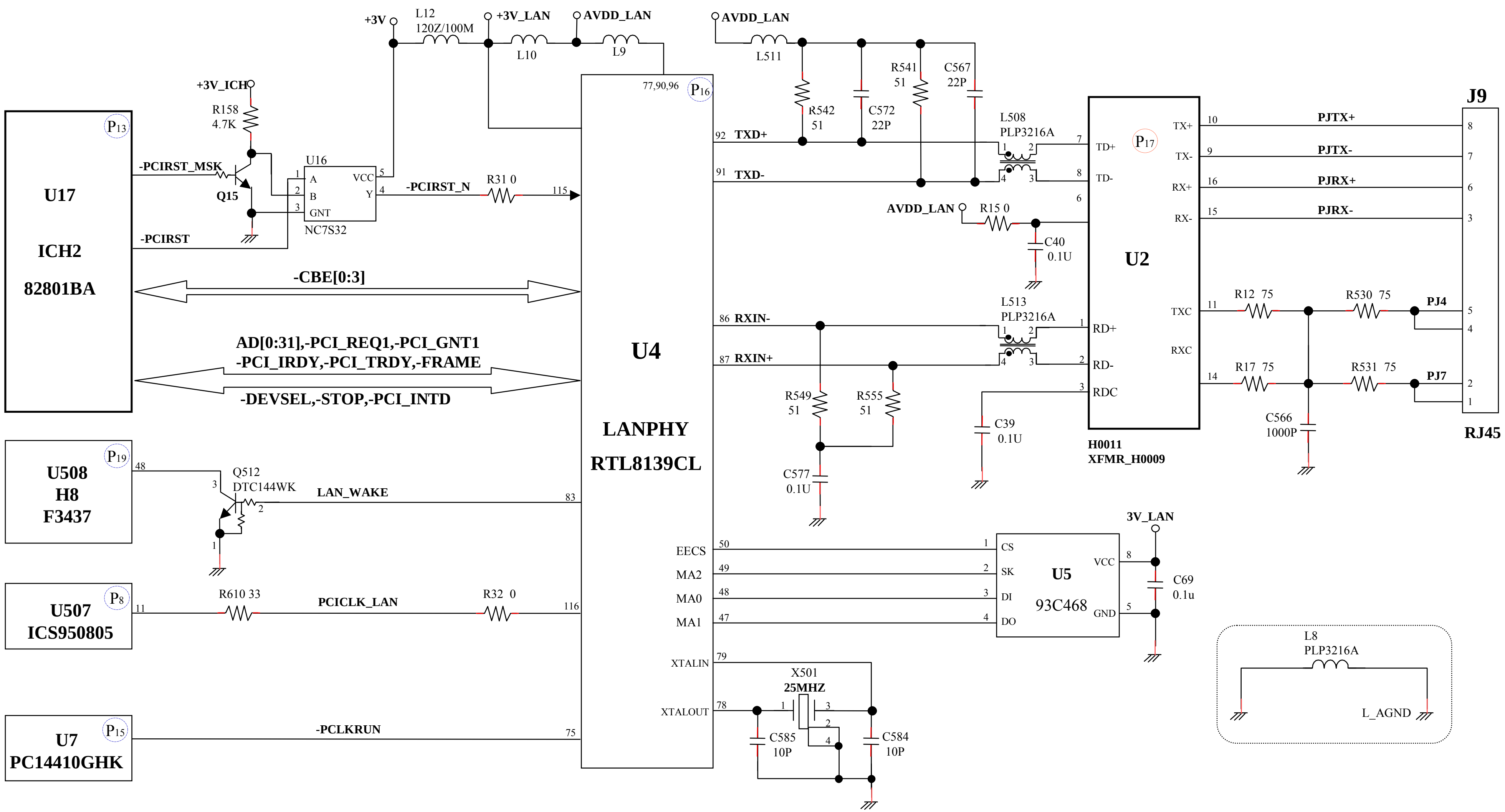
8.14 Audio Failure

No sound from speaker after audio driver is installed.



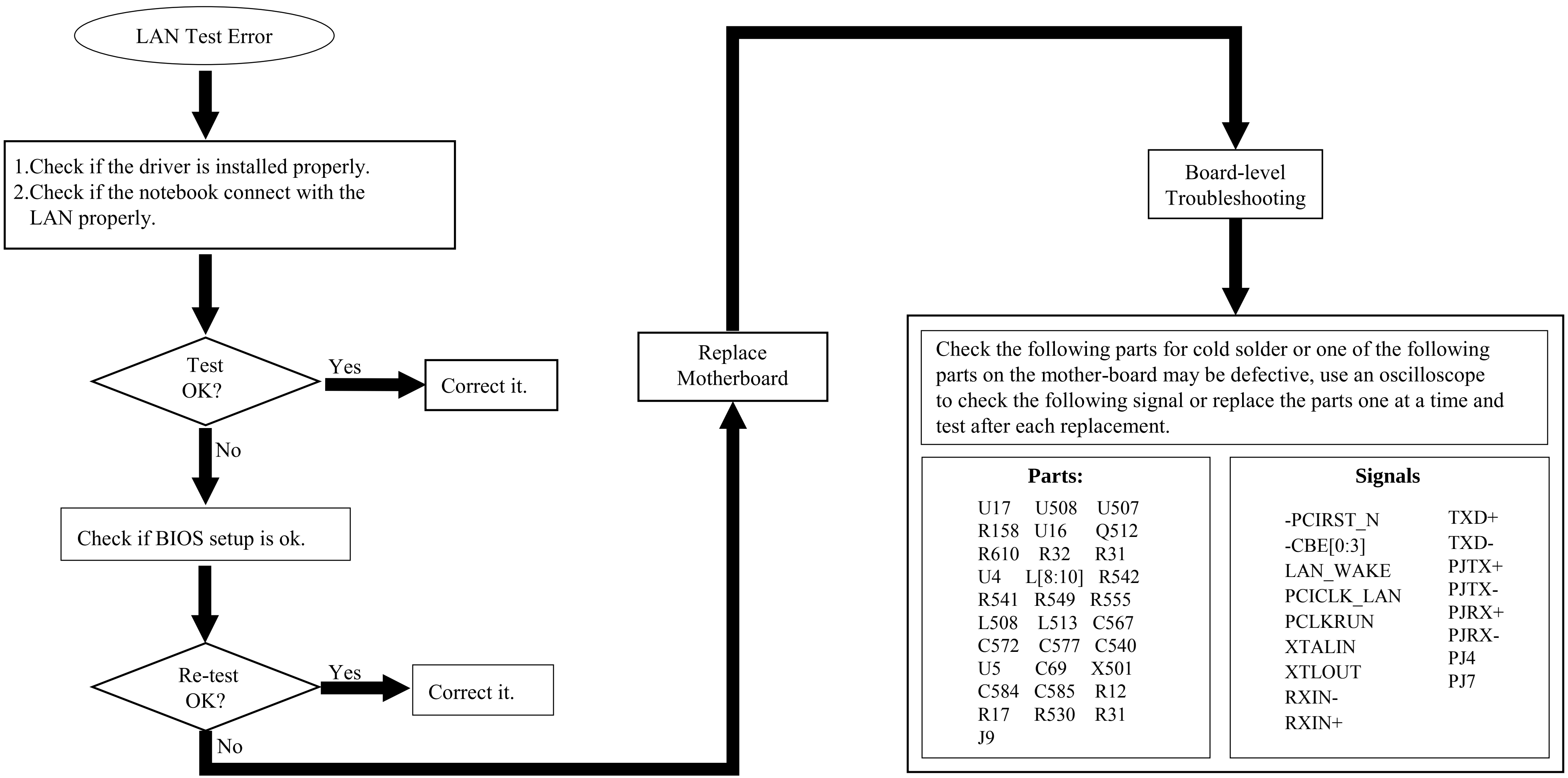
8.15 LAN Test Error

An error occurs when a LAN device is installed.



8.15 LAN Test Error

An error occurs when a LAN device is installed.



9. Spare Parts List -- recommend (1)

Category	Part Number	Description	Remark
CPU	324180786162	BFM-IPC;IC,CPU,WILLA	526267120029(1/15 Delete, The CPU not use in the part
SDRAM MODULE	323767120001	BFM-IPC;DRAM MODULE,	526267120029
COVER ASSY	340671200007	COVER ASSY; SPEAKER,8170	
	340671200007	COVER ASSY;KB,8170	
PCB;PWA-8170 TOUCHPAD BD	442164900010	TOUCH PAD MODULE;TM41PD-350	
	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENU	
HOUSING KIT	340671200002	COVER ASSY;8170	
	340671200006	COVER ASSY;RAM,8170	1/17 ECR:7939102700 delete
	340671200025	COVER ASSY;RAM-1,8170	1/17 ECR:7939102700 add
	343671200003	PLATE;KEYBOARD,8170	
	344669900003	COVER;HINGE,7170	
	421669900007	WIRE ASSY;TOUCHPAD,7170	
	340671200008	BRACKET ASSY;T-P,8170	
	340671200019	SPERKER ASSY;L,8170	
	340671200012	SPEAKER ASSY;R,8170	
	421671200031	MICROPHONE ASSY;8170	
	421671200008	WIRE ASSY;MDC,8170	
	340671200020	FAN ASSY;8170	
PWA;PWA-8170,MOTHER BD,T/U	411671200001	PWA;PWA-8170,MOTHER BD	
	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
	340671200003	HOUSING ASSY;8170	
BATT ASSY	442671200001	BATT ASSY;11.1V/6AH,LI-,PANASONI	

Category	Part Number	Description	Remark
PWA;PWA-8170,D/D BD,T/U	411671200004	PWA;PWA-8170,D/D BD,SMT	
	346671200011	INSULATOR;CD-ROM,M-B,8170	
	346671200036	INSULATOR,MDC,8170	
LCD ASSY	413000020305	BFM-IPC;LCD,UB141X01	526267120014,17,29
	413000020281	LCD;14X13-102,TFT,14	526267120037
	421671200002	WIRE ASSY;UNIPAC,14.	526267120014,17,29
	421671200001	WIRE ASSY;HYUNDAI,14	526267120037
	421671200007	WIRE ASSY;INVERTER,8170	
	340669900001	TILT UNIT;R,7170	
	340669900002	TILT UNIT;L,7170	
	340671200016	HOUSING ASSY;HANNSTER,14.1",LCD,	
	340671200017	HOUSING ASSY;UNIPAC,	526267120014,17,29
	340671200015	HOUSING ASSY;HYUNDAI	526267120037
	341669900004	BRACKET;LCD,14.1",HYUNDAI,L,7170	
	345669900004	RUBBER;LCD,DOWN,7170	
	345671200001	RUBBER;LCD,UP,8170	
	346664900010	FILM;LCD PROTEC,.14.2",235*300,5	
	340671200018	COVER ASSY;LCD,8170	
	341669900003	BRACKET;LCD,14.1,HYU	
	412671200001	PCB ASSY;INVERTER BD,11P,8170,MS	1/22 add option(7939102656
	412671300001	PCB ASSY;D/A BD,SUMIDA,STINGRAY	1/22 add option(7939102656
PWA;PWA-	411671200007	PWA;PWA-8170,ESB BD	
AC ADPT ASSY	442671200004	AC ADPT ASSY;19V/4.74A,DELTA,817	
	242670800113	BFM-WORLD MARK;WINXP,7521N	

9. Spare Parts List -- recommend (2)

Category	Part Number	Description	Remark
HDD ASSY;30G	344669900010	CASE;HDD,7170	
	523467120012	BFM-IPC;HDD DRIVE,30	526267120029
KBD	531066990001	KBD;86,US,K000918E1,7170	
	531020237308	KBD;87,FR,K000918F1,	526267120014
	531020237307	KBD;87,GR,K000918F1,	526267120017,29
AK;01-EN	332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
	332810000034	PWR CORD;250V/2.5A,2	526267120017
	332810000043	PWR CORD;250V/3A,2P,	526267120037
	421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
BEZEL ASSY;DVD ROM,QUANTA,	340669900046	BEZEL ASSY;DVD ROM,QUANTA,7170	
	343669900006	BRACKET;CD-ROM,7170	
	523430061901	DVD DRIVE;8X,SDR-081,H=12.7,QUAN	

9. Spare Parts List -- All (1)

Part Number	Description	Location(s)
441999900204	AC ADPT ASSY OPTION;8170	
442671200004	AC ADPT ASSY;19V/4.74A,DELTA,817	
541667120001	AK;01-EN,BOX,8170	
541667120032	AK;EN,8170,UTILITY ONLY	
441999900056	BATT ASSY OPTION;LI,9-CELL,8170	
442671200001	BATT ASSY;11.1V/6AH,LI-,PANASONI	
298000000002	BATTERY HOLDER;FOR CR2032,BH-800	BT1
338530010018	BATTERY; LI,3V/220MAH,CR-2032	BT1
340669900046	BEZEL ASSY;DVD ROM,QUANTA,7170	
242670800113	BFM-WORLD MARK;WINXP,7521N	
221669940001	BOX;AK,7170	
340671200008	BRACKET ASSY;T-P,8170	
343669900006	BRACKET;CD-ROM,7170	
341669900005	BRACKET;LCD,14.1",HANNSTAR,R,717	
341669900004	BRACKET;LCD,14.1",HYUNDAI,L,7170	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
421671000001	CABLE ASSY;USB FDD	
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C562,C576,C60,PC32,PC500
272072473402	CAP;.047U,16V ,10%,0603,X7R,SMT	C651
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C103,C104,C105,C109,C110,
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C501,C502,C507,C512,C513,
272003683401	CAP;0.068U,CR,25V,10%,0805,X7R	C701
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C1,C132,C141,C173,C174,C5
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C1,C4,PC18,PC517,PC518
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C500,C502,C566

Part Number	Description	Location(s)
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C688,C689,PC528
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C503,C504,C505,C506
272431105901	CAP;100U ,10V ,20%,7343,SMT	PC1,PC3,PC8
272431107509	CAP;100U,2V,20%,7343,SDK-CAP	C12,C28,PC572,PC573,PC57
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C101,C107,C108,C117,C134,
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C10,C11,C13,C14,C15,C17,C
272023106701	CAP;10U ,25V ,+80-20%,1210,Y5U,	PC20,PC28,PC541,PC544
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,S	C211,C212
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C556,C559
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C122,C142,C160,C163,C164,
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC2
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	C171,C522,C545,C681,PC51
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC505
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C183,C196,C622,C625,C646,
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C638,C65,C81
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C531
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C523,C524,C546,C547,C704
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C187,C197,C203,C205,C504,
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	C16,C49,C514,C552,C59,C61
272043226501	CAP;22U ,25V ,+-20%,1812,Y5U,SMT	PC505,PC506,PC507,PC513,
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C199,C46,C93
272431337506	CAP;330U,4V,20%,7343,SMT	PC7
272432336506	CAP;33U,16V,+-20%,7343,POSCAP,SM	C30,C31
272421336501	CAP;33U,TT,8V,20%,3528,SMT	C570,C571
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C125,C131,C153,C208,C35,C

9. Spare Parts List -- All (2)

Part Number	Description	Location(s)
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C182,C54,C587
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	PC501,PC511,PC514
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C611,C691,C692,C693,C694,
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC20
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C136,C139,C143,C149,C680,
272075509801	CAP;5P ,CR,50V,+ -.5PF,0603,NP	C617,C618
272075680302	CAP;68P ,50V ,5% ,0603,NPO,SMT	C630,C633
221668950010	CARD BOARD,BTM,PALLET,M722	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
221671220002	CARTON;NON-BRAND,MSL,8170	
431671200001	CASE KIT;8170	
344669900010	CASE;HDD,7170	
451669900051	CD ROM ME KIT;24X,7170	
273000500052	CHOKE COIL;0.7UH,1.6mOHM,25%,20A	PL1,PL2
273000500053	CHOKE COIL;10UH,21.6mOHM,5.4A	PL7
273000500053	CHOKE COIL;10UH,21.6mOHM,5.4A	PL1
273000111004	CHOKE COIL;160OHM/100MHZ,25%,321	L23,L24,L508,L513,L532,L53
273000111004	CHOKE COIL;160OHM/100MHZ,25%,321	L2,L3
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	L1
331000007009	CON;BAT,7P,2.5MM,CENLINK	J28
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J1
331720025005	CON;D,FM,25P,2.775,R/A	J1
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J11
291000144004	CON;FPC/FFC,20P*2,1.0MM,H=4.6,ST	J2

Part Number	Description	Location(s)
291000142404	CON;FPC/FFC,24P,1MM,H8.2,ST,ACES	J12
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J500
331040020004	CON;HDR,FM,10P*2,2.54MM,R/A,H8,4	J3
331030044013	CON;HDR,FM,22*2,2MM,ST,C16805	
331040050011	CON;HDR,FM,25P*2,1.27MM,R/A,HSG	J6
291000011024	CON;HDR,FM,5P*2,1.27MM,ST,H4.5,S	J501
331040020005	CON;HDR,MA,10P*2,2.54MM,R/A,H8.4	PJ1
291000011209	CON;HDR,MA,12P*1,1.25,ST,SMT	J6
291000024409	CON;HDR,MA,22P*2,2MM,R/A,SMT,ALL	J14
331040050009	CON;HDR,MA,25P*2,1.27MM,R/A,HSG	PJ2
331040050010	CON;HDR,MA,50P,0.8MM,R/A,H1.1	J10
291000011027	CON;HDR,MA,5P*2,1.27MM,ST,H17.5,	J5
291000020303	CON;HDR,SHROUD,MA,3P,1.25MM,R/A,	J502
291000256823	CON;IC CARD PART;68P,0.635,H5,SM	J8
331000004018	CON;IEEE1394,MA,4P,.8MM,R/A,LINK	J21
331870004017	CON;MINI DIN,4P,R/A,W/GROND,C108	J4
331810006044	CON;PHONE JACK,6P2C,H11.5,RJ11,T	J13
291000810806	CON;PHONE JACK,8P8C,SMD,RJ45	J9
331840010005	CON;POF MINI JACK,10P,W/SPDIF,2F	J19
331910003039	CON;POWER JACK,3P,D=2.0,SINGATRO	J5
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J22
331000004025	CON;USB,MA,R/A,4P*1,2MM,85116-40	J2,J3
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J16,J18,J20,J4
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J7
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J501

9. Spare Parts List -- All (3)

Part Number	Description	Location(s)
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J15
345669600065	CONDUCTIVE TAPE;MB,SDRAM,RACE	
340671200007	COVER ASSY; SPEAKER,8170	
340671200002	COVER ASSY;8170	
340671200001	COVER ASSY;ID1,8170	
340671200009	COVER ASSY;KB,8170	
340671200018	COVER ASSY;LCD,8170	
340671200006	COVER ASSY;RAM,8170	
344671000001	COVER;FOR 7170;USB FDD	
344669900003	COVER;HINGE,7170	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP500,CP501,CP502,CP503,
291006214438	DIMM SOCKET;144P,.8MM,H4,SX6E,HR	J505
291006214439	DIMM SOCKET;144P,.8MM,H4,SX6ER,H	J503
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD503
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D501
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D10,D16
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D509,D510
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	PD2,PD3
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1,D3,D4,D6
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D501,D502,D503,D504,D505
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D502,D503
288100056003	DIODE;BAW56,70V,215MA,SOT-23	PD500,PD502
288100056003	DIODE;BAW56,70V,215MA,SOT-23	PD502
288101003001	DIODE;EC10QS03L,30V,1A,SMT	D508,D513
288101003001	DIODE;EC10QS03L,30V,1A,SMT	PD503,PD504

Part Number	Description	Location(s)
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	D500
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	PD1
288103103001	DIODE;EC31QS03L,30V,3A,SMT	PD1,PD2,PD4,PD5,PD6
288103103001	DIODE;EC31QS03L,30V,3A,SMT	PD4,PD5,PD6
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D5,D7
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100036001	DIODE;RLZ3.6B,ZENER,3.45V,5%,SMT	D8
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	PD7
344670500042	DUMMY CARD;PCMCIA,TETRA	
523430061901	DVD DRIVE;8X,SDR-081,H=12.7,QUAN	
523467120011	DVD ROM ASSY;8X,SDR-081,QUANTA,8	
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C166
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC18,PC23,PC46,PC47
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC11,PC19,PC4,PC5,PC9
272601227501	EC;220U ,10V,M,6.3*7.7,-15+105',	C204,C210
312278206152	EC;820U ,4V,+-20%,10X10.5,FPCAP	PC3,PC5,PC6,PC7
227669900005	END CAP; HEATSINK, AK BOX,7170	
227671200001	END CAP;8170	
227669900004	END CAP;BATTERY,7170	
227669900002	END CAP;FDD,FRAME,7170	
227669900003	END CAP;FDD,T/B,7170	
481671200002	F/W ASSY;KBD CTRL,8170	U508
481671200001	F/W ASSY;SYS/VGA BIOS,8170	U12
340671200020	FAN ASSY;8170	
523411442052	FD DRIVE;1.44M,3.5",D353FU,MITSU	

9. Spare Parts List -- All (4)

Part Number	Description	Location(s)
523499993004	FDD DRIVER OPTION;EXT. FDD,7170	
523467100002	FDD KIT;D353FUE,FOR 7170,USB,MSL	
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN	FA501
273000610014	FERRITE ARRAY;60OHM/100MHZ,3216,	FA500
273000610014	FERRITE ARRAY;60OHM/100MHZ,3216,	RP1,RP2,RP3,RP4
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L500,L501,L502,L520,PL8
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L508,L510
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L505,PL10,PL11,PL14,PL15,
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L1,L4,L507,L509,PL2,PL3,PI
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L10,L11,L12,L13,L14,L15,L1
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L502,L503,L504,L505
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L523,L524,L525,L527,L528,I
273000150022	FERRITE CHIP;60OHM/100MHZ,2012,S	L17,L18,L19
273000150022	FERRITE CHIP;60OHM/100MHZ,2012,S	L501
422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENU	
346664900010	FILM;LCD PROTEC,.14.2",235*300,5	
341671200009	FINGER;EMI GROUND SMD FINGER,H=2	E1,E2,E3,E4,E5,E500,E502,I
341671200010	FINGER;EMI GROUND SMD FINGER,H=4	E501,E509,E510,E513
341671200010	FINGER;EMI GROUND SMD FINGER,H=4	E501
342600001203	FINGER;EMI GROUNDING SMD FINGER,	E514,E515
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U1
295000010044	FUSE;1.1A/6V,POLY SWITCH,1210,SM	F500,F501,F502
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,PF2
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF501
346671200026	GASKET;1394,M/B,8170	

Part Number	Description	Location(s)
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U5
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U9
283450083002	IC;FLASH,512K*8-70,PLCC32,ST39SF	
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
284582801027	IC;ICH2,82801BA,BGA421	U17
284595080001	IC;ICS950805,200MHZ,TSSOP56	U507
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU513
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	PU7
286329510001	IC;LP2951CM-3.3,VOLTAGE REGULATO	PU510
286317099001	IC;LTC1709-9,PWM,QSOP,36P	PU508
286301632002	IC;MAX1632CAI,PWM CTRL,SSOP,28P	PU1
286301772001	IC;MAX1772,PWM,QSOP,28P	PU511
286133078001	IC;MC33078D,LOW NOISE OP AMP.,SO	U513
286305248002	IC;MIC 5248-1.2BM5,LV12,LDO REG,	U501
284500006003	IC;MOBILTY RADEON M6-D,BGA484	U516
281300732001	IC;NC7S32,SINGLE OR GATE,SC70-5	U16,U510
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70	U8
286307805010	IC;NJM78L05UA,VOL REGULATOR,SOT,	U511
286302040002	IC;P2040B,LCD PANEL EMI,S0,8P	U503
284501284001	IC;PAC1284-01Q,TERMIN. NETWK,QSO	U501,U502
284587393002	IC;PC87393F,TQFP,100P	U509
284504410005	IC;PCI4410A,CARDBUS/OHCI,uBGA,20	U7
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U2
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ3,PQ510,Q505
286300055001	IC;TC55,3.3V,250mA,REG.,SOT89	PU8

9. Spare Parts List -- All (5)

Part Number	Description	Location(s)
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U18
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U504
284500411001	IC;TSB41AB1,1394 PHY,PQFP,64P	U14
273000114002	INDUCTER;4.7UH,10%,1206,SMT	L509,L512
273000990023	INDUCTOR;10UH,CDRH125B,SMT	PT1
273000150106	INDUCTOR;4.7UH,10%,2012,SMT	L2,L3
346671200036	INSULATOR,MDC,8170	
346671200011	INSULATOR;CD-ROM,M-B,8170	
346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	
346669900004	INSULATOR;INVERTER,7170	
346671200007	INSULATOR;PCMCIA,8170	
346671200008	INSULATOR;RTC,8170	
531099990101	KBD OPTION;86,US,7170	
531066990001	KBD;86,US,K000918E1,7170	
451671200052	LABEL KIT;N-B,8170	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242662300009	LABEL;25*10MM,3020F	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242671200004	LABEL;AGENCY-GLOBAL,MSL,8170	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900012	LABEL;BAR CODE,32x11MM,7170	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	

Part Number	Description	Location(s)
242669900005	LABEL;LCD SIDE,7170	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
441671200004	LCD ASSY;HANNSTAR,SXGA+,14.1",81	
451671200004	LCD ME KIT;HANNSTAR,SXGA+,14.1",	
413000020290	LCD;HSD141PK11-A,TFT,14.1",SXGA+	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D11,D12,D13,D14,D15
344671000003	LENS;HOUSING,USB FDD	
526267120001	LTXNX;8170/4BCI/30C/1US1/18D3A/X	
561567120001	MANUAL KIT;EN,8170,N-B	
561567120013	MANUAL;USER'S,EN,8170,N-B	
421671200031	MICROPHONE ASSY;8170	
416267120004	NB PF;HANNSTAR,SXGA+,14.1",8170	
375102030010	NUT-HEX;M2,2,NIW	
375120262008	NUT-HEX;M2.6,NCG	
461671200002	PACKING KIT;N-B,8170	
227669900006	PAD;LCD/KB,ANIT-STATIC,7170	
221669950004	PARTITION;A,PALLET,7170	
221669950001	PARTITION;AK BOX,7170	
221669950005	PARTITION;B,PALLET,7170	
412671200001	PCB ASSY;INVERTER BD,11P,8170,MS	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
316671200003	PCB;PWA-8170 TOUCHPAD BD	R01
316671200002	PCB;PWA-8170/DD BD	R01
316671200005	PCB;PWA-8170/ESB BD	R01
316671200001	PCB;PWA-8170/M BD	R01

9. Spare Parts List -- All (6)

Part Number	Description	Location(s)
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U18
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U504
284500411001	IC;TSB41AB1,1394 PHY,PQFP,64P	U14
273000114002	INDUCTER;4.7UH,10%,1206,SMT	L509,L512
273000990023	INDUCTOR;10UH,CDRH125B,SMT	PT1
273000150106	INDUCTOR;4.7UH,10%,2012,SMT	L2,L3
346671200036	INSULATOR,MDC,8170	
346671200011	INSULATOR;CD-ROM,M-B,8170	
346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	
346669900004	INSULATOR;INVERTER,7170	
346671200007	INSULATOR;PCMCIA,8170	
346671200008	INSULATOR;RTC,8170	
531099990101	KBD OPTION;86,US,7170	
531066990001	KBD;86,US,K000918E1,7170	
451671200052	LABEL KIT;N-B,8170	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242662300009	LABEL;25*10MM,3020F	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242671200004	LABEL;AGENCY-GLOBAL,MSL,8170	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242669900012	LABEL;BAR CODE,32x11MM,7170	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	

Part Number	Description	Location(s)
242669900005	LABEL;LCD SIDE,7170	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
441671200004	LCD ASSY;HANNSTAR,SXGA+,14.1",81	
451671200004	LCD ME KIT;HANNSTAR,SXGA+,14.1",	
413000020290	LCD;HSD141PK11-A,TFT,14.1",SXGA+	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D11,D12,D13,D14,D15
344671000003	LENS;HOUSING,USB FDD	
526267120001	LTXNX;8170/4BCI/30C/1US1/18D3A/X	
561567120001	MANUAL KIT;EN,8170,N-B	
561567120013	MANUAL;USER'S,EN,8170,N-B	
421671200031	MICROPHONE ASSY;8170	
416267120004	NB PF;HANNSTAR,SXGA+,14.1",8170	
375102030010	NUT-HEX;M2,2,NIW	
375120262008	NUT-HEX;M2.6,NCG	
461671200002	PACKING KIT;N-B,8170	
227669900006	PAD;LCD/KB,ANIT-STATIC,7170	
221669950004	PARTITION;A,PALLET,7170	
221669950001	PARTITION;AK BOX,7170	
221669950005	PARTITION;B,PALLET,7170	
412671200001	PCB ASSY;INVERTER BD,11P,8170,MS	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
316671200003	PCB;PWA-8170 TOUCHPAD BD	R01
316671200002	PCB;PWA-8170/DD BD	R01
316671200005	PCB;PWA-8170/ESB BD	R01
316671200001	PCB;PWA-8170/M BD	R01

9. Spare Parts List -- All (7)

Part Number	Description	Location(s)
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R502
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R5,R537
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR562
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR557,R55,R56,R585,R586,R
271071334301	RES;330K ,1/16W,5% ,0603,SMT	R689
271071333101	RES;33K ,1/16W,1% ,0603,SMT	PR547
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R4,R5
271071374211	RES;37.4K,1/16W,1% ,0603,SMT	PR15
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R521
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	PR23,PR24,PR572,R158,R19
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR18,R124,R587
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R16,R8,R82
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR568
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	PR571
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R581
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R156,R157,R682,R683,R684,
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR16,R1,R501,R642,R646
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR4,PR5,PR506
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R619
271071475311	RES;475K ,1/16W,1% ,0603,SMT	PR564
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR553,R102,R42,R43,R579,R
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR9,R3,R6
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R520,R527,R528,R529,R535,
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR516,PR542
271071499011	RES;499 ,1/16W,1% ,0603,SMT	R14

Part Number	Description	Location(s)
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R582,R71
271071511812	RES;51.1,1/16W,1% 0603,SMT	R507,R508,R510,R512,R513,
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R103,R105,R106,R115
271071561101	RES;560 ,1/16W,1% ,0603,SMT	PR20
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	R104
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	PR519,R151,R24,R27,R550,R
271071620102	RES;62,1/16W,1% 0603,SMT	R2,R3,R506,R517
271071681101	RES;680 ,1/16W,1% ,0603,SMT	R522
271071683301	RES;68K ,1/16W,5% ,0603,SMT	R148
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R12,R17,R514,R530,R531
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R107,R108,R117,R118,R154,
271071841101	RES;845 ,1/16W,1% ,0603,SMT	R533
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP521
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP508
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP510
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP2,RP505
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP518
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP511
271611473301	RP;47K*4 ,8P ,1/16W,5% ,0612,SMT	RP520
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP512,RP515
271611682301	RP;6.8K*4,8P ,1/16W,5% ,0612,SMT	RP1,RP506,RP507,RP509
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP501
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP501
271621822302	RP;8.2K*8,10P,1/32W,5% ,1206,SMT	RP15,RP16,RP17,RP18
345671000001	RUBBER FOOT;HOUSING,USB FDD	

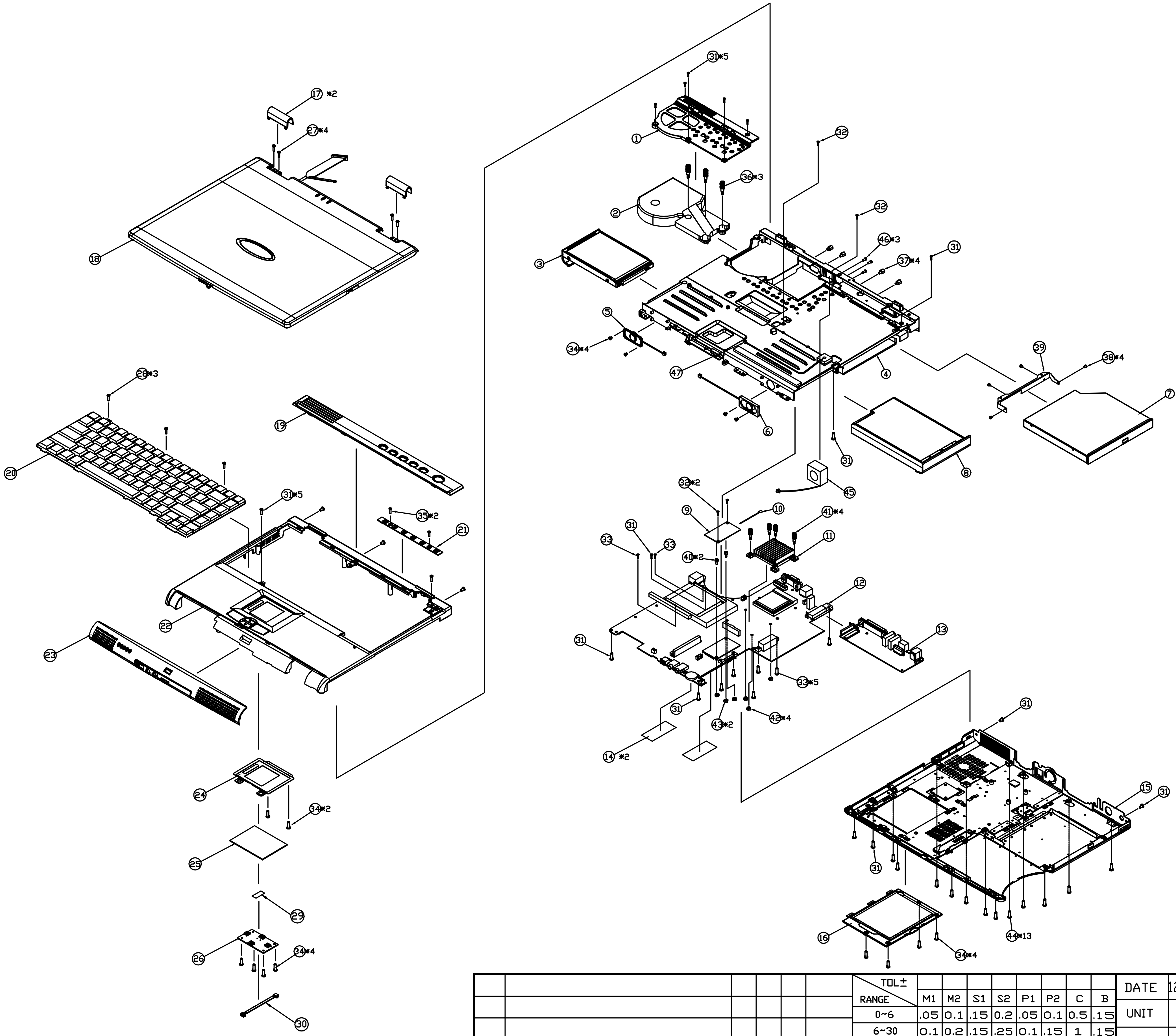
9. Spare Parts List -- All (8)

Part Number	Description	Location(s)
345669900004	RUBBER;LCD,DOWN,7170	
345671200001	RUBBER;LCD,UP,8170	
565167120001	S/W;CD ROM,SYSTEM,8170	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
340671200013	SCREW ASSY;CPU,8170	
340671200014	SCREW ASSY;IC,82845,8170	
371102011502	SCREW;M2L15,FLT(+),NIW/NLK	
323760000002	SDRAM MODULE;256M,8M*16,PC133,SP	
340671200005	SHIELDING ASSY;TOP,8170	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102010309	SPC-SCREW;M2L3.0,NIW/NLK,HD07	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370102010608	SPC-SCREW;M2L6,KD,HD φ 3 ,NIB/NL	
370102010606	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NL	
370102010605	SPC-SCREW;M2L6,NIW,HDT=0.4,779	

Part Number	Description	Location(s)
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
340671200012	SPEAKER ASSY;R,8170	
340671200019	SPERKER ASSY;L,8170	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
341668300008	STANDOFF;MDC MODEM,NLK,HOPE	
297040105012	SW;PUSH BUTTOM,4P,SP,12V/50MA,H2	SW1,SW2,SW3,SW4,SW5,SW
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW1,SW2,SW3,SW4
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	SW6
346671200002	THERMAL PAD;HEATSINK,CPU,8170	
310111103012	THERMISTOR;10K,1%,RA,0603,1P	R4
340669900002	TILT UNIT;L,7170	
340669900001	TILT UNIT;R,7170	
442164900010	TOUCH PAD MODULE;TM41PD-350	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ500,PQ501,PQ506,PQ507
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ1,PQ3
288203400001	TRANS;AO3400,N-MOSFET,SOT-23	Q13,Q503
288203401001	TRANS;AO3401,P-MOSFET,SOT-23	PQ1,PQ512,Q1,Q509
288204400001	TRANS;AO4400,N-MOSFET,SO-8	PU13,Q500,U505
288204400001	TRANS;AO4400,N-MOSFET,SO-8	PU501,PU504
288200144002	TRANS;DTA144WK,PNP,SMT	Q514
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ511,Q10,Q15,Q2,Q506,Q5
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ2,PQ509,Q12,Q14,Q3,Q4,
288200302001	TRANS;FDV302P,P-CHANNEL,SOT23	Q7
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	PQ505

9. Spare Parts List -- All (9)

Part Number	Description	Location(s)
288202303001	TRANS;SI2303DS,P-MOSFET,SOT-23	PQ2
288104362001	TRANS;SI4362DY,N-HOSFET,S08	PU1,PU2,PU501,PU502,PU5
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU5
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU503,PU506
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU6
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU502,PU505
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PU10,PU11,PU512,PU9
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ502,PQ503
288204892001	TRANS;SI4892DY,N-MOSFET,SO8	PU500,PU503,PU506,PU507
273001050065	TRANSFORMER;10/100 BASE,LF-H72P,	U2
373101710301	T-SCREW;I,M1.7,L3,K-HD,D3.0,NIB	
373002010002	T-SCREW;S.M2 L4, PAN(+),NIW	
373002010003	T-SCREW;S.M2 L5, PAN(+),NIW	
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S500
271911103906	VR;10K,20%,0.05W,RN101GAC10KPGJ-	VR1
421671200004	WIRE ASSY;HANNSTAR,14.1",SXGA,LC	
421671200007	WIRE ASSY;INVERTER,8170	
421671200008	WIRE ASSY;MDC,8170	
421669900007	WIRE ASSY;TOUCHPAD,7170	
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X502
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X503
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X1,X2
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X501
274012700401	XTAL;27MHZ,20PPM,16PF,7*5,4P,SMT	X500
274013276114	XTAL;32.768KHZ,10PPM,12.5PF	X3



ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
47	421671200031	MICROPHONE ASSY;8170	1	
46	371102011502	SCREW;M2L15,FLT(+),NIW/NLK	3	
45	340671200020	FAN ASSY;8170	1	
44	370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	13	
43	375102030010	NUT-HEX;M2,2,NIW	3	
42	375120262008	NUT-HEX;M2.6,NCG	4	
41	340671200014	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NLK	4	
40	341668300008	STANDOFF;MDC MODEM,NLK,HOPE	2	
39	343669900006	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	1	
38	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	4	
37	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	
36	340671200013	SCREW ASSY;CPU,8170	3	
35	370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	2	
34	370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	14	
33	370102010606	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NLK	7	
32	370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	4	
31	270102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	18	
30	421669900007	WIRE ASSY;TOUCHPAD,7170	1	
29	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	1	
28	370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	3	
27	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	
26	411671200006	PWA;PWA-8170,T/P BD	1	
25	442164900010	TOUCH PAD MODULE;TM41PD-350	1	
24	340671200008	BRACKET ASSY;T-P,8170	1	
23	340671200007	COVER ASSY; SPEAKER,8170	1	
22	340671200002	COVER ASSY;8170	1	
21	411671200007	PWA;PWA-8170,ESB BD	1	
20	531066990001	KBD;86,US,K000918E,7170	1	
19	344671200003	COVER;KEYBOARD,8170	1	
18	441671200001	LCD ASSY;HYUNDAI,XGA,14.1",8170	1	OPTION
17	344669900003	COVER;HINGE,7170	2	
16	340671200006	COVER ASSY;RAM,8170	1	
15	340671200003	HOUSING ASSY;8170	1	
14	346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	2	
13	411671200004	PWA;PWA-8170,D/D BD,T/U	1	
12	411671200001	PWA;PWA-8170,MOTHER BD	1	
11	343671200011	HEATSINK;IC,82845,8170	1	
10	421671200008	WIRE ASSY;MDC,8170	1	
9	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	
8	441999900056	BATT ASSY OPTION;LI,9-CELL,8170	1	
7	523467120005	CD ROM ASSY;24X,224E-B92,TEAC,8170	1	
6	340671200012	SPEAKER ASSY;R,8170	1	
5	340671200019	SPERKER ASSY;L,8170	1	
4	340671200005	SHIELDING ASSY;TOP,8170	1	
3	523467120001	HDD ASSY;10G,2.5",9.5MM,8170	1	
2	340671200010	HEATSINK ASSY;CPU,8170	1	
1	343671200003	PLATE;KEYBOARD,8170	1	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /

TOL± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	12/10/2001	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	— —	DRAWING NAME	NB PF;UNIPAC,XGA,14.1",8170		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	461267120001	R00

MiTAC International Corp.

SHEET NO. 1 OF 1

MODEL : 8170 Revision 02

Contexts

DRAW	DESIGN	CHECK	ISSUED

History of Schematics

Revision 0A (EVT)

1.ADD 1UF FOR ADM1021A Temperature Monitor.
2.DEL EMAIL BTN SW5 AND D16 LED INCICATOR.
3.+1.8VA CHANGE (+1.8V_ICH) FOR ICH2.
4.+3VA CHANGE (+3V_ICH) FOR ICH2.
5.-PCIRST CONTROL HDD & CD_ROM RESET,CHANGE VON GPIO PIN EACH RESET FOR S3 WEAKUP.
6.ADD TWO 10K PULL_UP RESISTOR FOR H8 THERMAL SENSE ,TWO FAN FREEBACK SCHEMATIC.
7.ADD U515 & CHANGE J5 FOR 8170 QK/B AND 8175 LED/B COMMON.
8.ADD -LID PIN ON J6 FOR 8175 COVER SWITCH.
9.MODIFY TOUCH_PAD +5VS CHANGE +5VS.
10.MODIFY LANPHY +3VS CHANGE +3V.
11.MODIFY ICH2 +5VA CHANGE +5V.
12.MODIFY RTC CIRCUITRY +3VA CHANGE +5VA VON 330K & 1M DIVIDER.

Revision 0B (DVT)

1.ADD DIODE FOR S.B +5VS DRAIN.
2.ADD C717 &C718 (4.7U) for boot time "popo"tone.
3.ADD R162 modify 2M BIOS pull +5VS.
4.Change SDRAM Q8 for IO_DATA ram module.
5.ADD 1U CAP for inverter RED too light.
6.IEEE1394 modify 1394_GND of digital GND for ESD issue.
7.MDC modify to digital GND.
8.Modify FAN feedback +5V change +5VS and FAN control pin modify +5VS change +5V.
9.Second fan modify connect Vertical to Horizontally.

Revision 01 (PVT)

1.CHANGE CAP 0.068U OF 0603 TO 0805.
2.LAN OF MA8(PIN61) PULL HI +3V.
3.R163,R164,R696,R697,L535 CHANGE OF DFS FOR COST DOWN.
4.AMP(MUTE IN) ADD PULL HI +5VS.
5.LCD CONNECT PROVISION 5P CAP.

POWER STATES

STATE / SIGNAL	VOTAGE	FULL ON	STR	STD	MEC-OFF	REMARK
-SUSB	-	HIGH	LOW	LOW	LOW	
-SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
RTC_VCC	+3.3V	O	O	O	O	
CPU_CORE	+1.75V	O	X	X	X	
+1.8VS	+1.8V	O	X	X	X	
+1.8V_ICH	+1.8V	O	O	X	X	
VDDR_MEM2.5	+2.5V	O	X	X	X	
+3VS	+3.3V	O	X	X	X	
+3V	+3.3V	O	O	X	X	
+3V_ICH	+3.3V	O	O	X	X	
+5VS	+5V	O	X	X	X	
+5V	+5V	O	O	X	X	
+5VA	+5V	O	O	0	0	
+12VS	+12V	O	X	X	X	
+12V	+12V	O	O	X	X	

IDSEL

IDSEL	CHIP
AD18	
AD11	
AD18	LAN
AD19	PCMCIA

BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	PCMCIA
-REQ1/-GNT1	LAN
-REQ2/-GNT2	
-REQ3/-GNT3	NU
-REQ4/-GNT4	NU

PCIINT

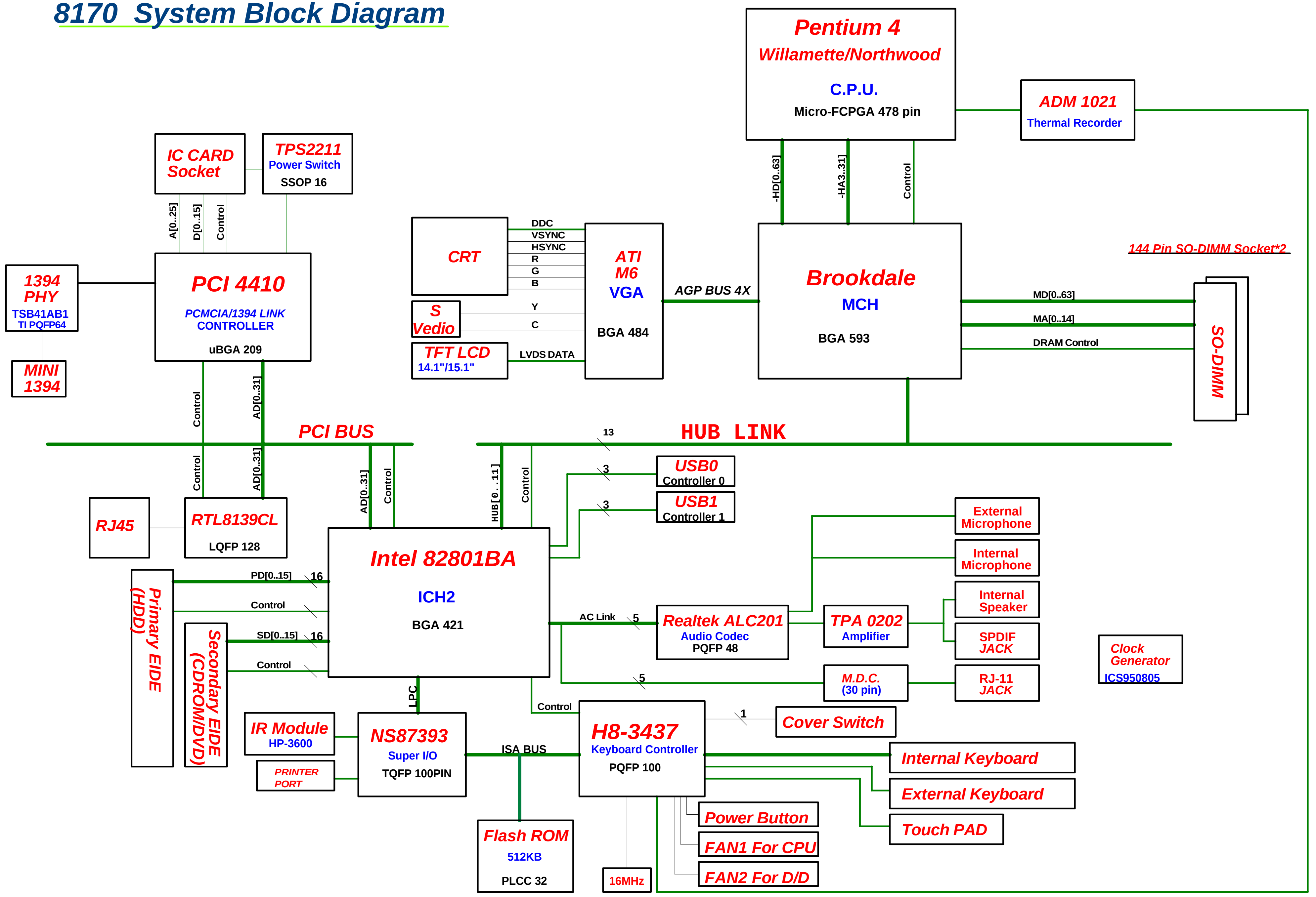
PCIINT	CHIP
INTA	PCMCIA/ATI VGA
INTC	PCMCIA/1394
INTH	USB2
INTD	USB1/LAN

1	COMP
2	GND
3	IN-1
4	GND
5	POWER
6	IN-2
7	GND
8	SOLDER

MiTAC

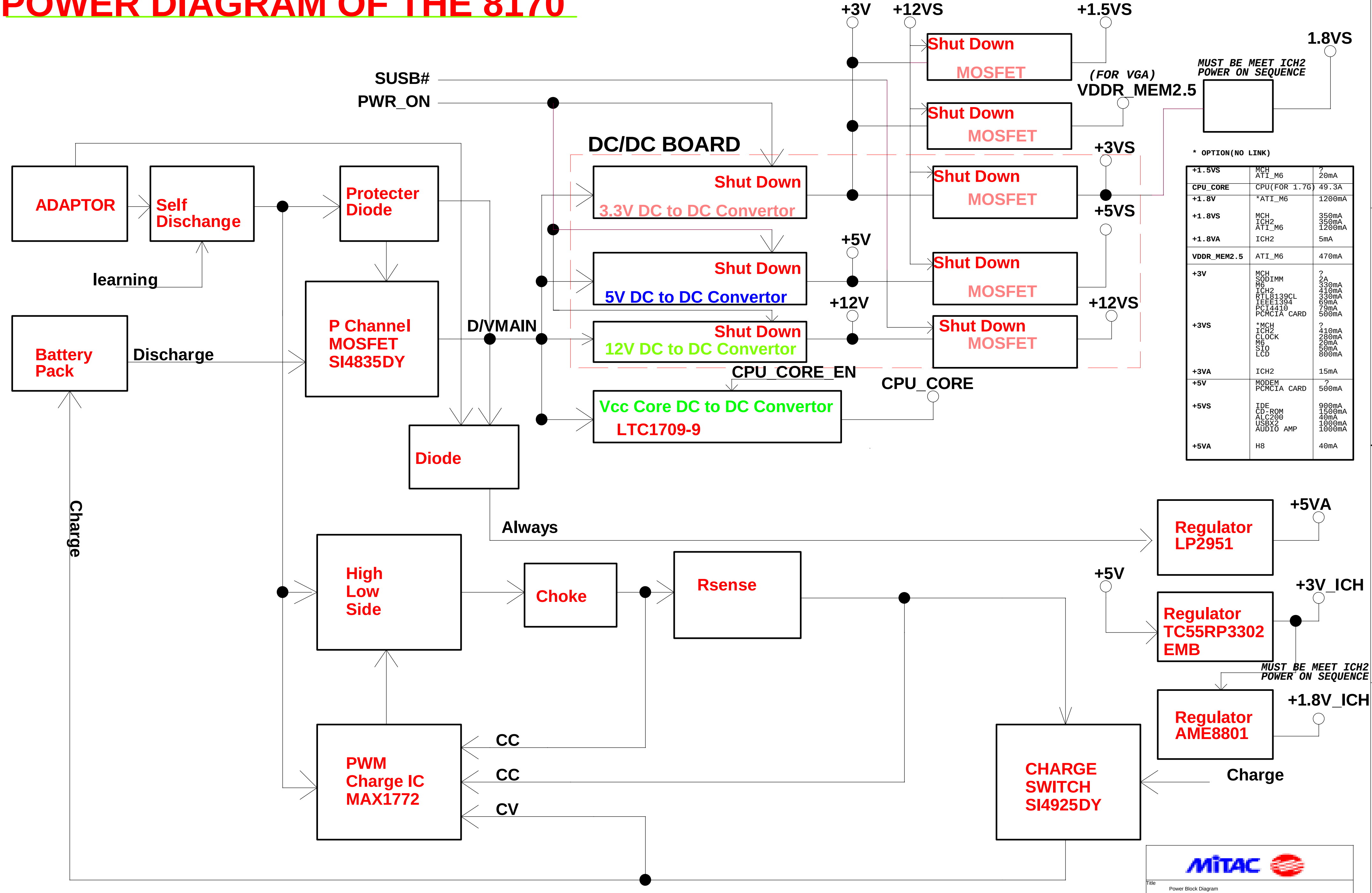
Title	Cover Sheet		
Size C	Document Number 411671200001		Rev 02
Date: Friday, December 28, 2001	Sheet 1	of 22	

8170 System Block Diagram



MiTAC			
Title: System Block Diagram			
Size	Document Number 411671200001		Rev 02
Date: Friday, December 28, 2001	Sheet 2 of 22		

POWER DIAGRAM OF THE 8170

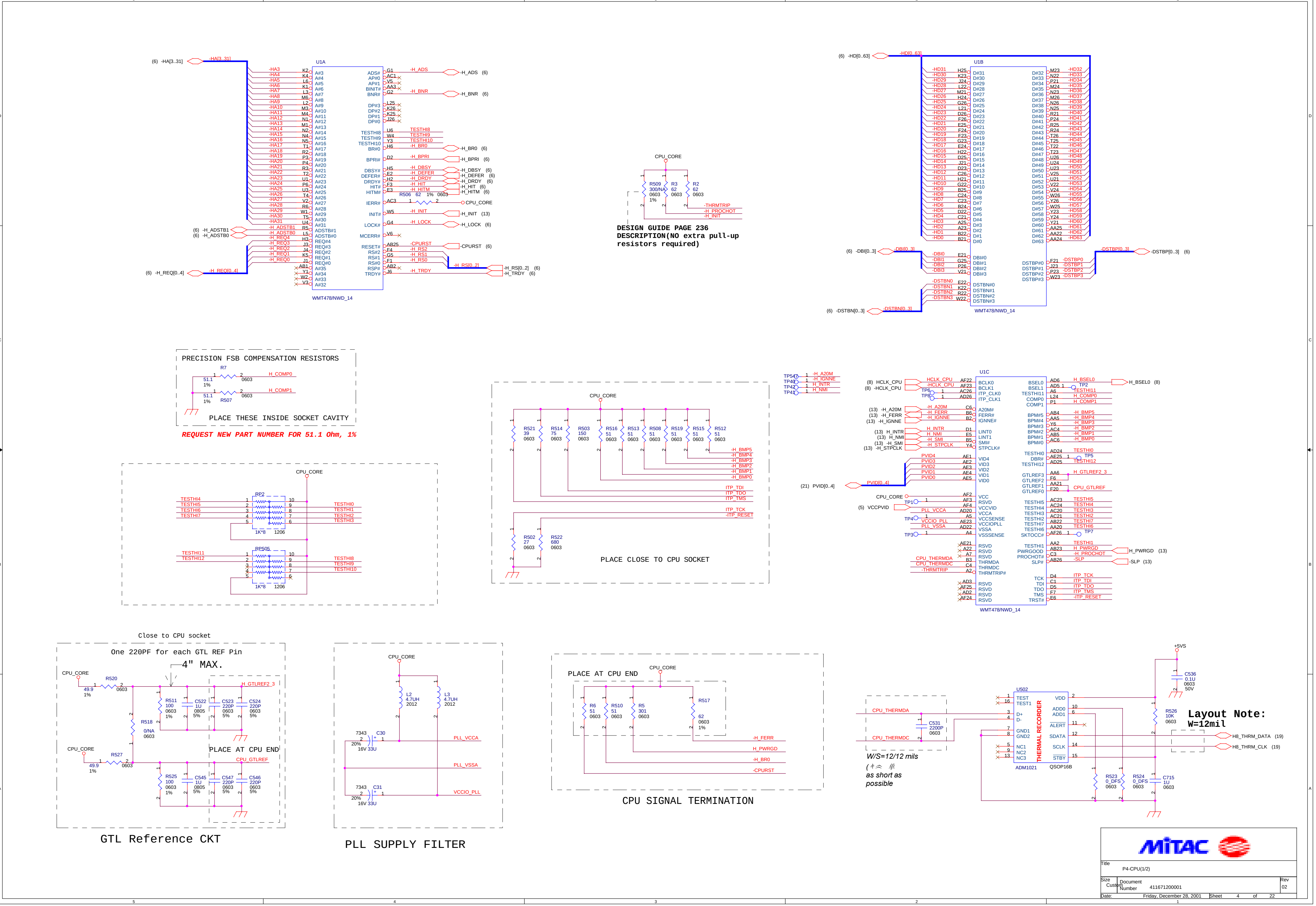


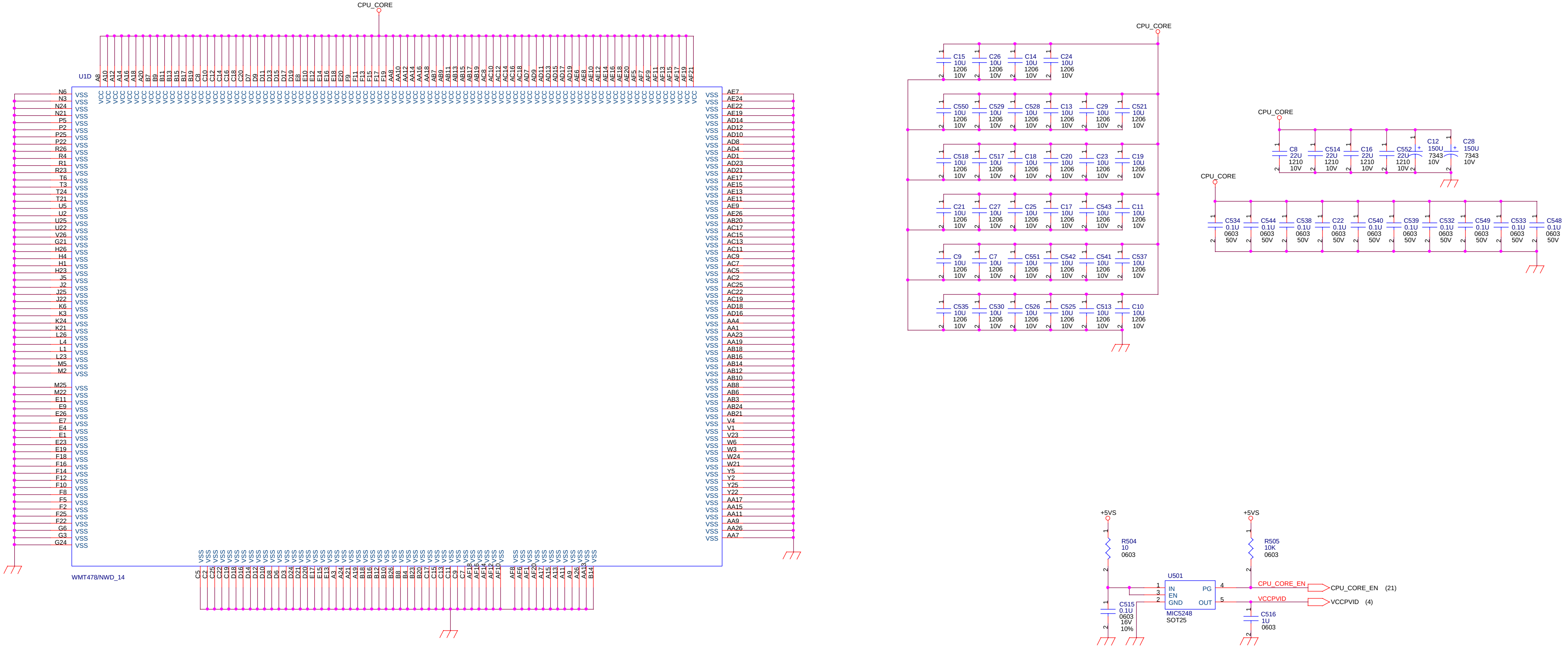
* OPTION(NO LINK)

+1.5VS	MCH ATI_M6	? 20mA
CPU_CORE	CPU(FOR 1.7G)	49.3A
+1.8V	*ATI_M6	1200mA
+1.8VS	MCH ICH2 ATI_M6	350mA 350mA 1200mA
+1.8VA	ICH2	5mA
VDDR_MEM2.5	ATI_M6	470mA
+3V	MCH SODIMM M6 ICH2 RTL8139CL IEEE1394 PCI4410 PCMCIA CARD	? 2A 330mA 410mA 330mA 69mA 79mA 500mA
+3VS	*MCH ICH2 CLOCK M6 SIO LCD	? 410mA 280mA 20mA 50mA 800mA
+3VA	ICH2	15mA
+5V	MODEM PCMCIA CARD	? 500mA
+5VS	IDE CD-ROM ALC200 USBX2 AUDIO AMP	900mA 1500mA 40mA 1000mA 1000mA
+5VA	H8	40mA

MiTAC

Title	Power Block Diagram	
Size	Document Number 411671200001	Rev 02
Date: Friday, December 28, 2001	Sheet 3 of 22	

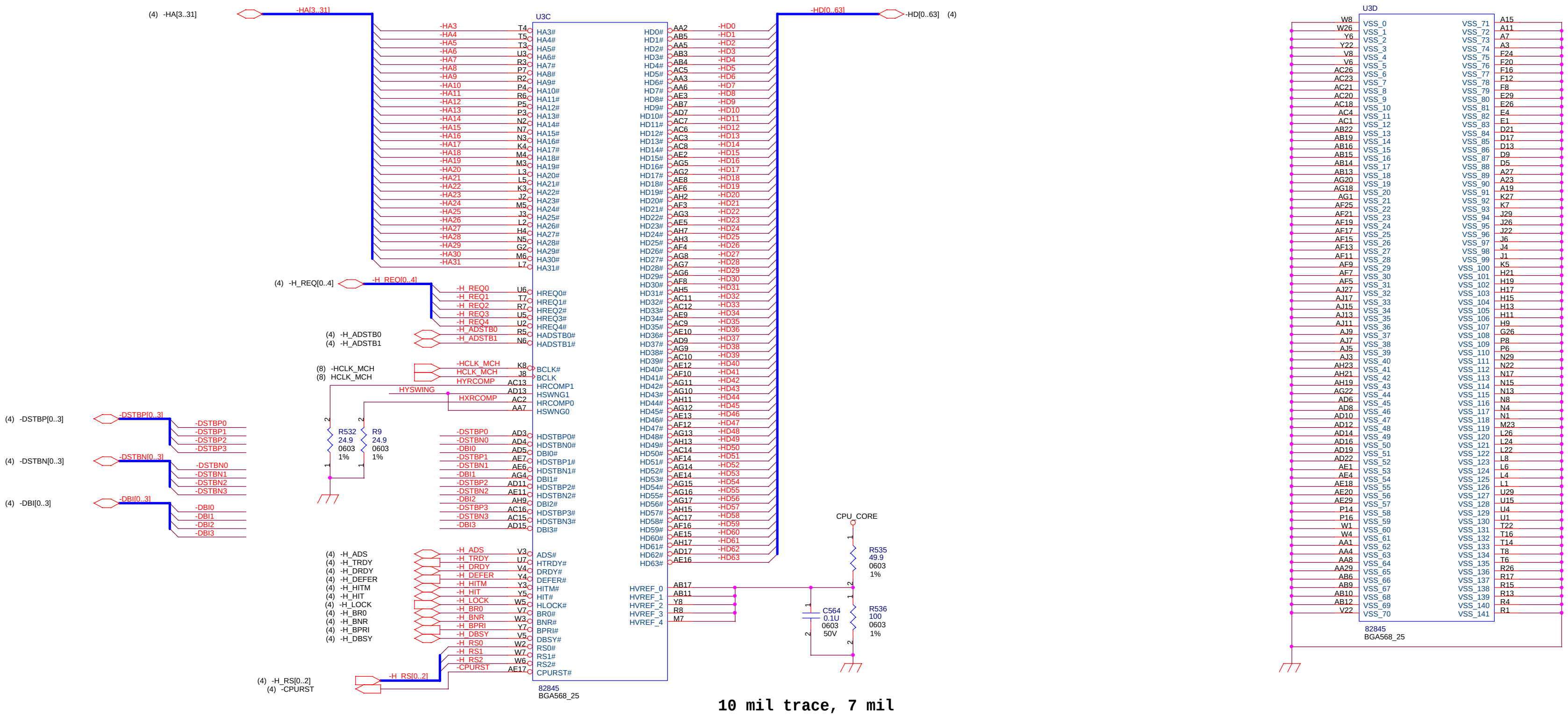

PRECISION FSB COMPENSATION RESISTORS
PLACE THESE INSIDE SOCKET CAVITY
REQUEST NEW PART NUMBER FOR 51.1 Ohm, 1%
DESIGN GUIDE PAGE 236
DESCRIPTION(NO extra pull-up
resistors required)
PLACE CLOSE TO CPU SOCKET
Close to CPU socket
One 220PF for each GTL REF Pin
4" MAX.
PLACE AT CPU END
GTL Reference CKT
PLL SUPPLY FILTER
PLACE AT CPU END
CPU SIGNAL TERMINATION
THERMAL RECORDER
W/S=12/12 mils
as short as
possible
Layout Note:
W=12mil
U1A
U1B
U1C
U502
ADM1021
QSOP16B
WMT478/NWD_14
CPU_CORE
+5VS
H8_THRM_DATA (19)
H8_THRM_CLK (19)
MITAC
Title
P4-CPU(1/2)
Size
Custom
Document
Number
411671200001
Rev
02
Date:
Friday, December 28, 2001
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Title: P4-CPU(2/2)

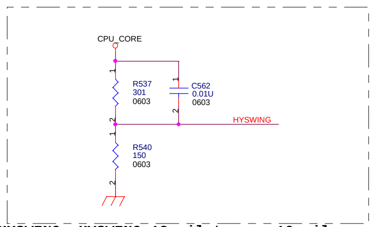
Size: Custom | Document Number: 411671200001 | Rev: 02

Date: Friday, December 28, 2001 | Sheet 5 of 22



10 mil trace, 7 mil space, Cap place near MCH and between two resistors.

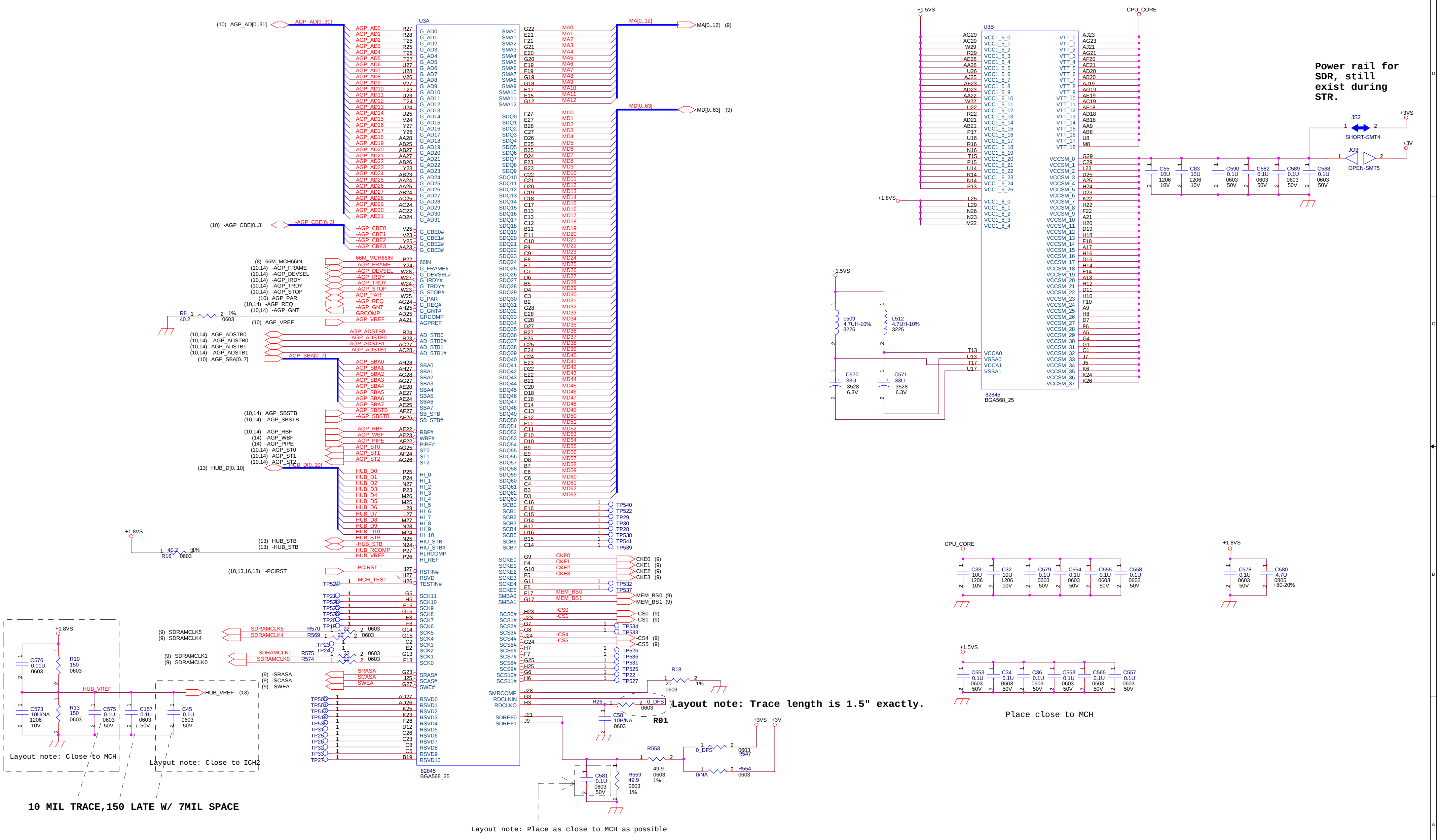
PLACE AT MCH845 END



HXSWING, HYSWING 12 mil trace, 10 mil space

MiTAC

Title	Brookdale-MCH845(1/2)
Size Custom	Document Number 411671200001 — Rev 02
Date:	Friday, December 28, 2001 — Sheet 6 of 22



MiTAC

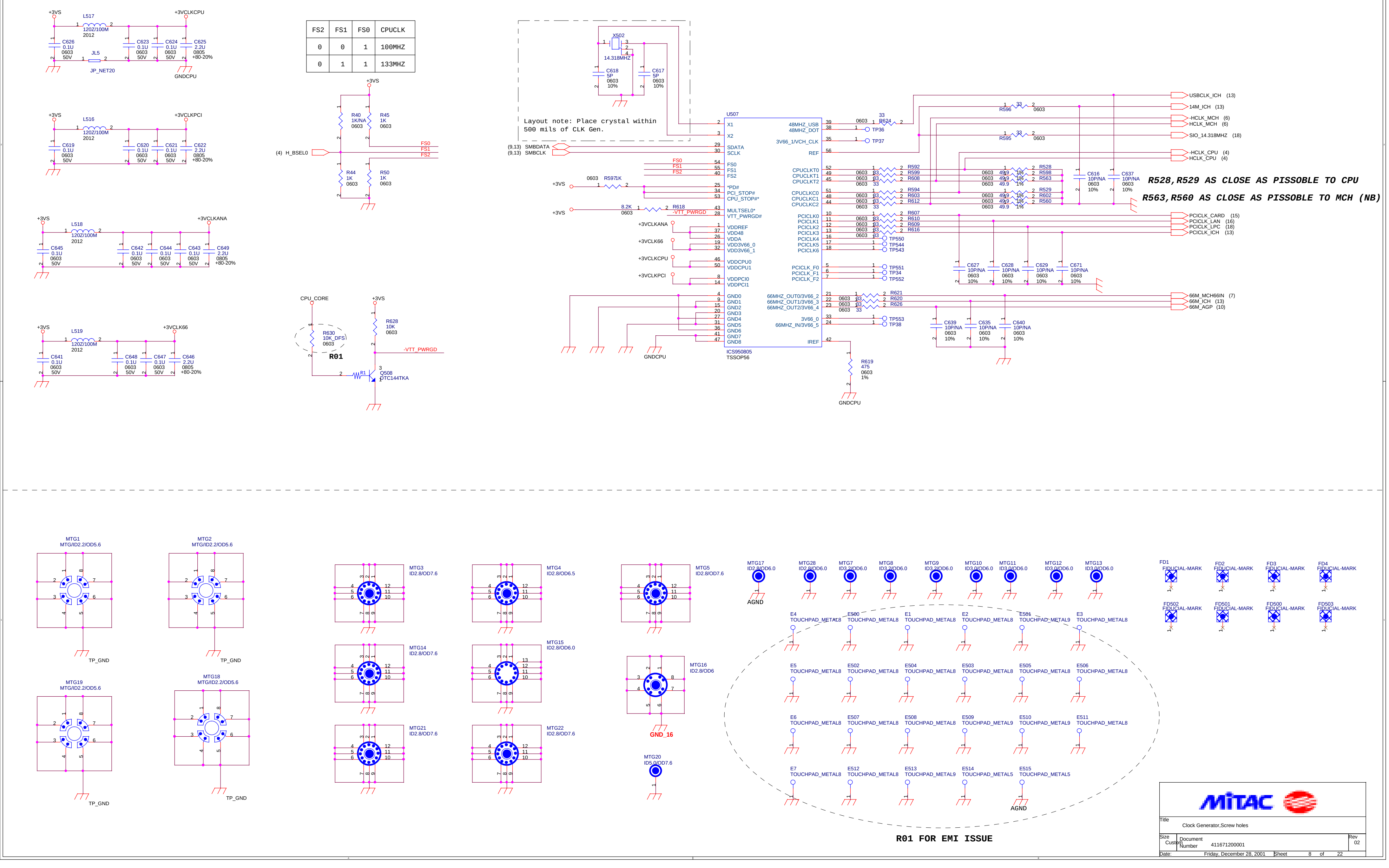
Title
Brookdale-MCH845(2/2)

Size	Document Number	Rev
Custom	411671200001	02

Date: Friday, December 28, 2001 Sheet 7 of 22

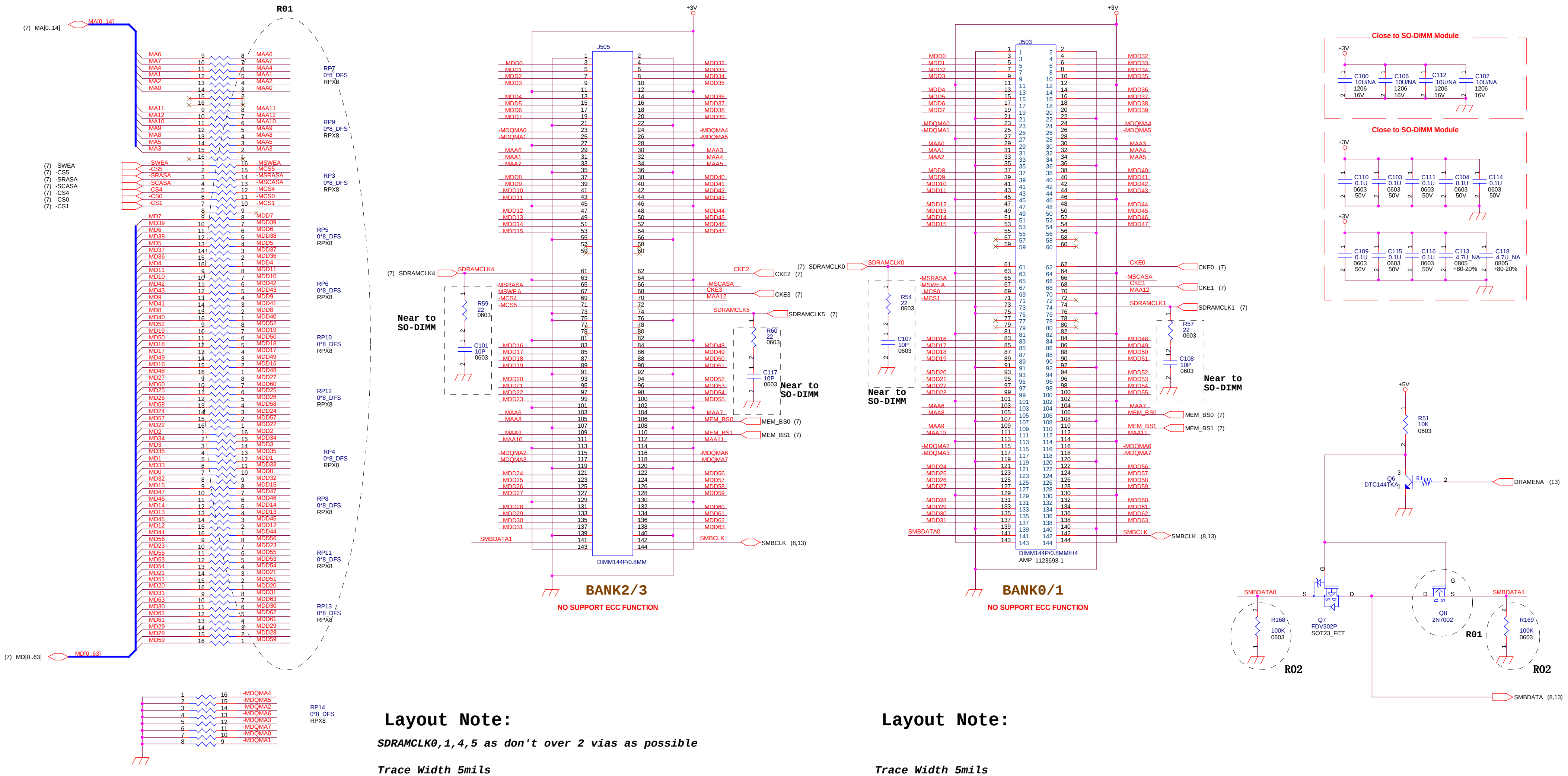
CLOCK GENERATOR

FS2	FS1	FS0	CPUCLK
0	0	1	100MHZ
0	1	1	133MHZ



SYSTEM MEMORY

SO-DIMM Module



Layout Note:

SDRAMCLK0,1,4,5 as don't over 2 vias as possible

Trace Width 5mils
Trace Spacing 12mils
Group Spacing (spacing from other signal groups) 12mils

MCH	Data signals 2"<L1<4"	DIMM1	Data signals 0.4"<L2<0.6"	DIMM2

Layout Note:

Trace Width 5mils
Trace Spacing 12mils
Group Spacing (spacing from other signal groups) 12mils

MCH	-SCS[0..11],SCKE[0..7] SMA[0..12],SBS]0..1] SRAS#,SCAS#,SWE# 2"<L1<3"	DIMM1	-SCS[0..11],SCKE[0..7] SMA[0..12],SBS]0..1] SRAS#,SCAS#,SWE# 0.4"<L2<0.6"	DIMM2

MiTAC

Title	SO-DIMM Memory X 2
Size / Document Number	411671200001
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GPIO [13:0:] have internal pull-down

GPIO[1:0] - AGP skew straps : allow for the adjustment of the phase between AGP 1X CLK and PCICLK.

GPIO[3:2] - X1CLK_skew straps : allow for the adjustment of the phase between X1CLK and X2CLK.

GPIO[6:4] - Bus configuration straps : This straps are controlling the bus type, the clock PLL select and the IDSEL. Default is [000] - AGP 4X.

GPIO[7] - VGA disable : default position is 0 (ie. VGA enable)

GPIO[8] - ID disable : left open in normal operation

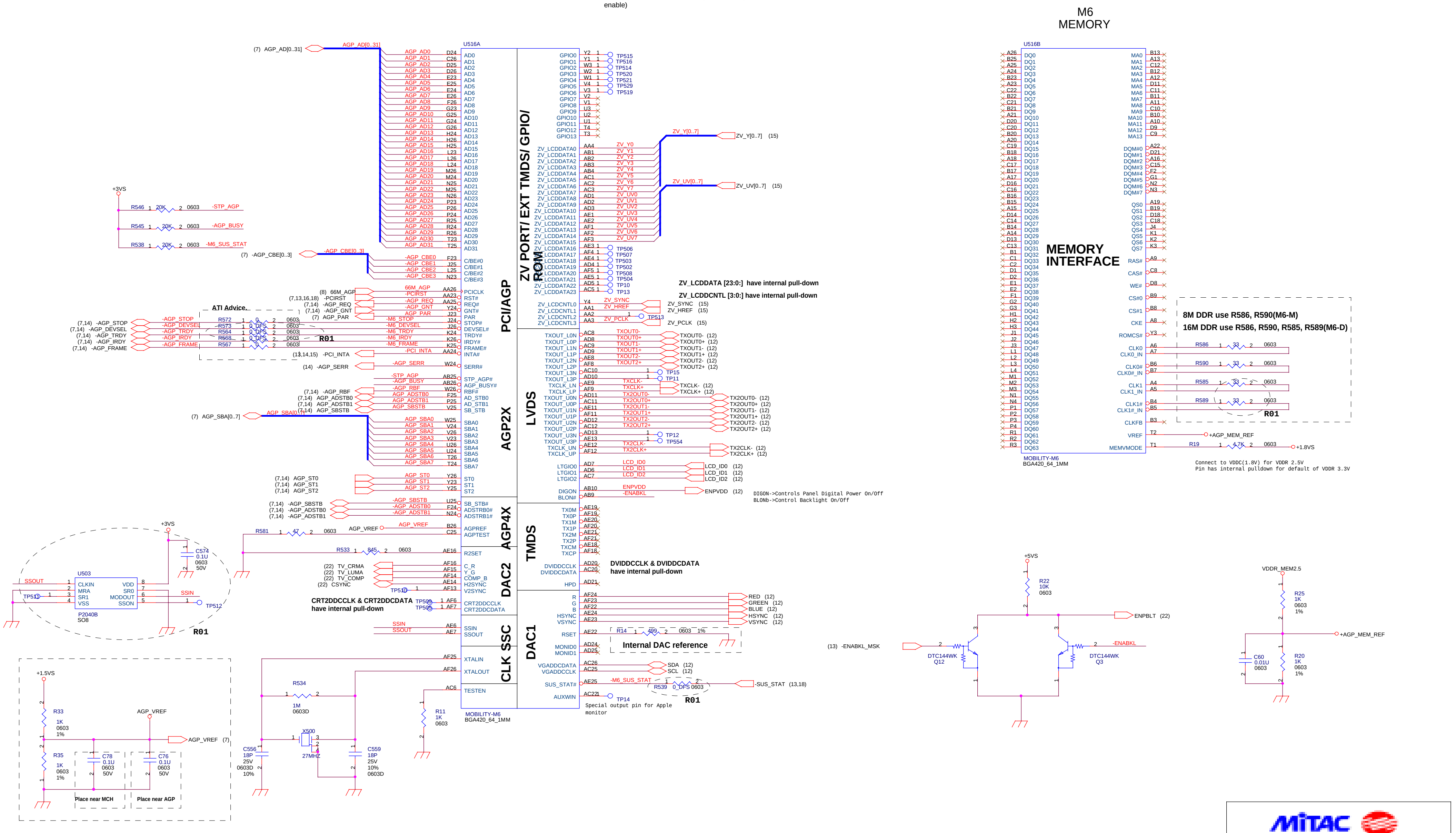
GPIO[9] - External I2C : Data

GPIO[10] - External I2C : CLK

GPIO [10:9] for external ROM or capture use.

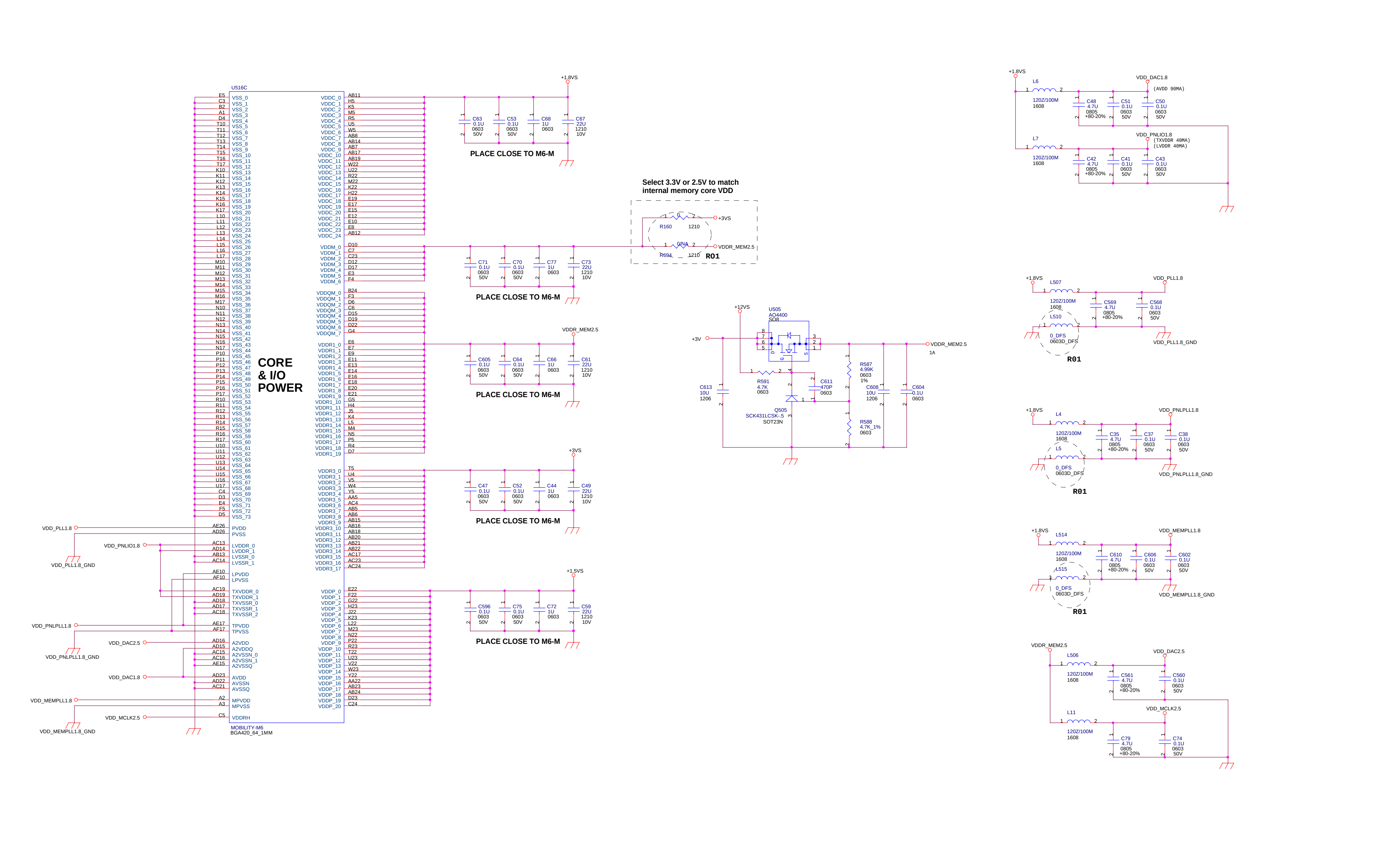
GPIO[13:11] - ROMIDCFG Straps : If the graphic subsystem has no ROM attached, these straps serve for controlling the chip ID.

M6
MEMORY



MiTAC

Title	VGA-M6(1/2)
Size Custom	Document Number 411671200001
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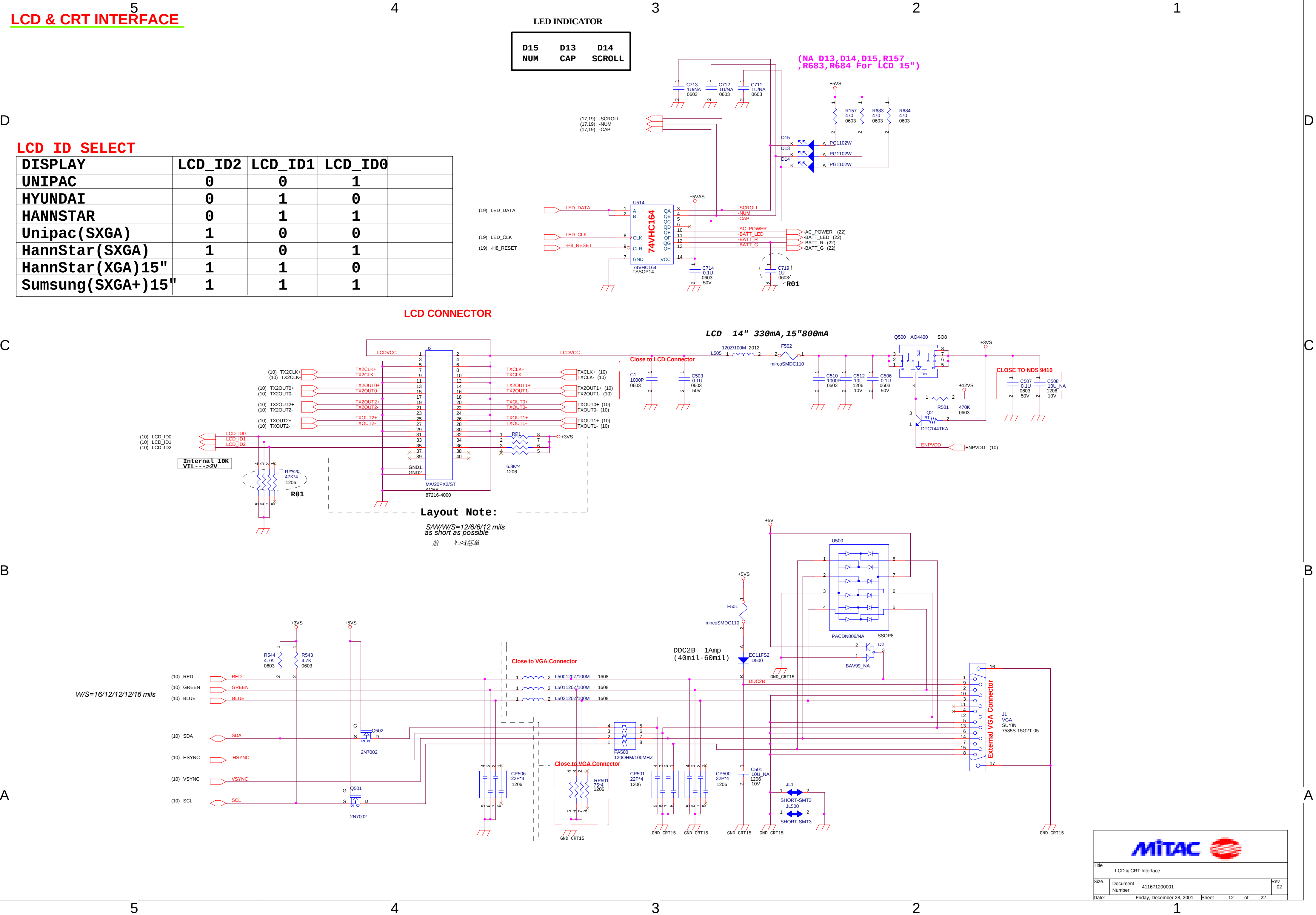
Title VGA-M6(2/2)

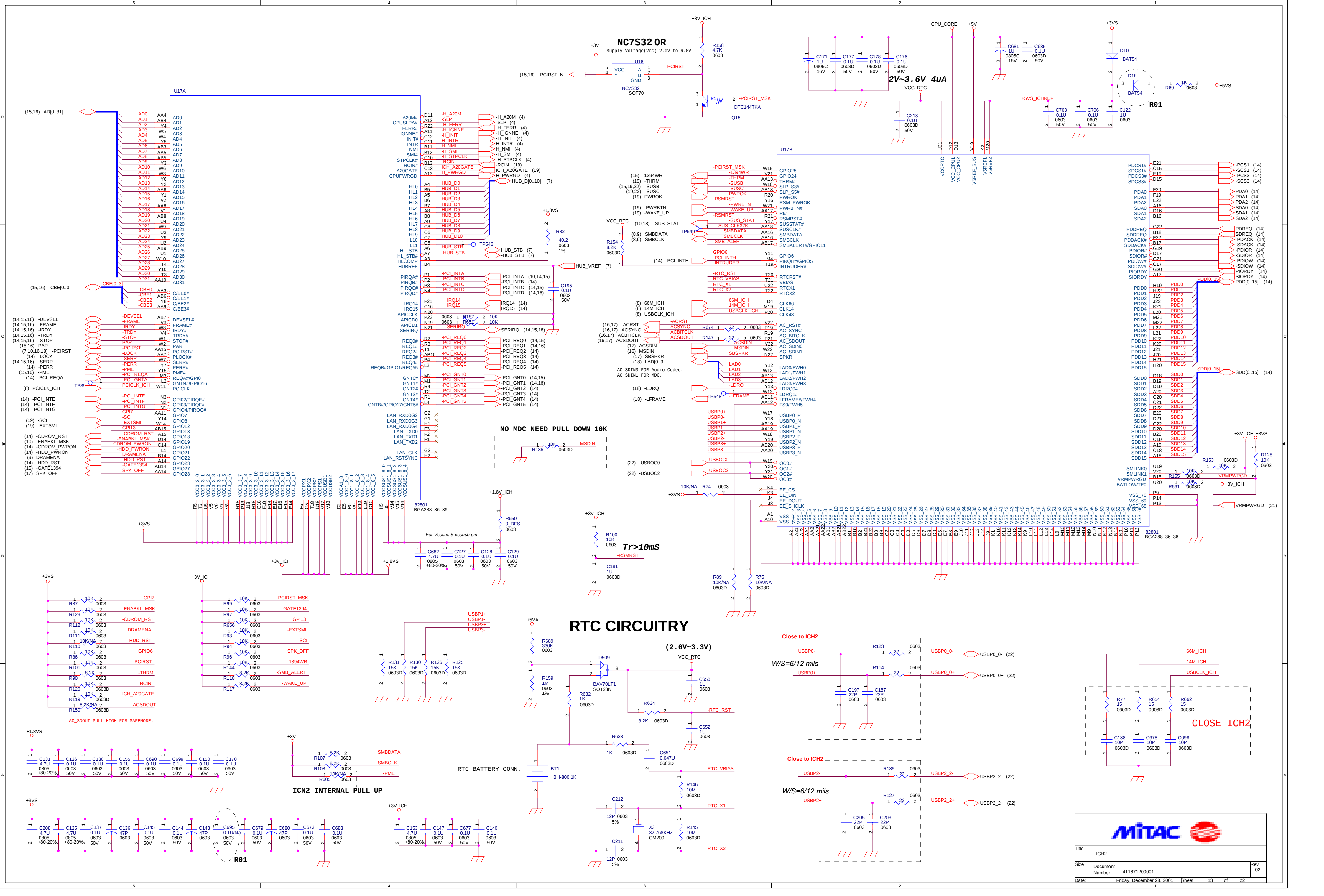
Size	Document Number	411671200001	Rev 02
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LCD & CRT INTERFACE

LCD ID SELECT

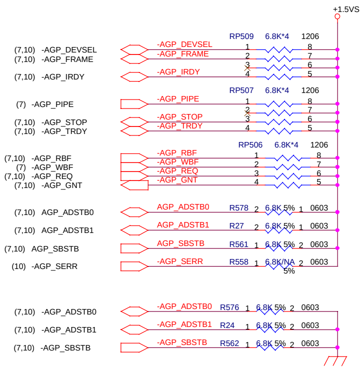
DISPLAY	LCD_ID2	LCD_ID1	LCD_ID0
UNIPAC	0	0	1
HYUNDAI	0	1	0
HANNSTAR	0	1	1
Unipac(SXGA)	1	0	0
HannStar(SXGA)	1	0	1
HannStar(XGA)15"	1	1	0
Sumsung(SXGA+)15"	1	1	1

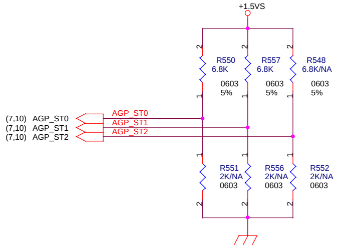



NC7S32 OR
Supply Voltage(Vcc) 2.0V to 6.0V
U16
NC7S32
SOT70
Q15
DTC144TKA
U17A
82801
BGA288_36_36
U17B
2V~3.6V 4uA
R01
NO MDC NEED PULL DOWN 10K
For Vccsus & vccusb pin
Tr>10mS
AC_SDIN0 FOR Audio Codec.
AC_SDIN1 FOR MDC.
AC_SDOUT PULL HIGH FOR SAFEMODE.
ICN2 INTERNAL PULL UP
RTC CIRCUITRY
(2.0V~3.3V)
RTC BATTERY CONN.
BT1
BH-800.1K
D509
BAV70LT1
SOT23N
X3
32.768KHZ
CM200
Close to ICH2
W/S=6/12 mils
CLOSE ICH2
MITAC
Title
ICH2
Size
Document Number
411671200001
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AGP BUS

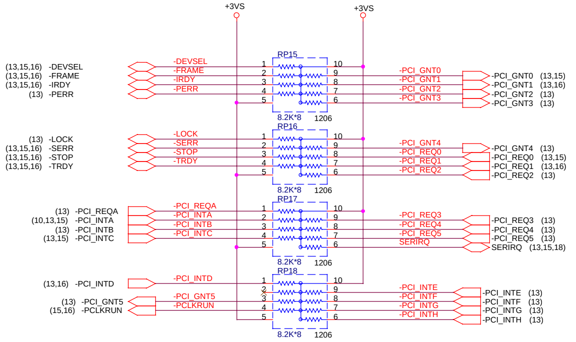
AGP_ST1	AGP_ST0	MCH STRAP
X	0	DDR
X	1	SDR
0	X	533MHZ
1	X	400MHZ



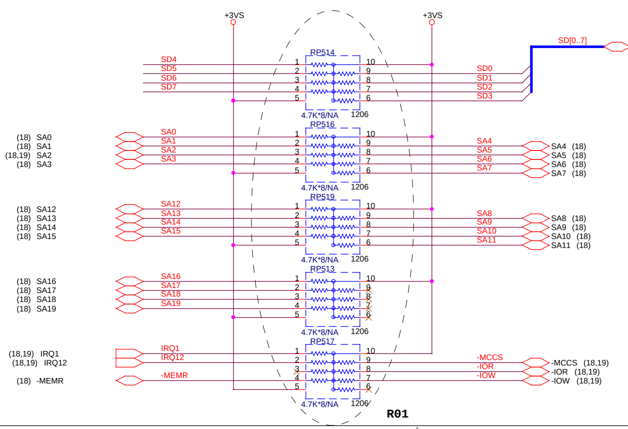


PLACE CLOSE TO VGA

PCI BUS

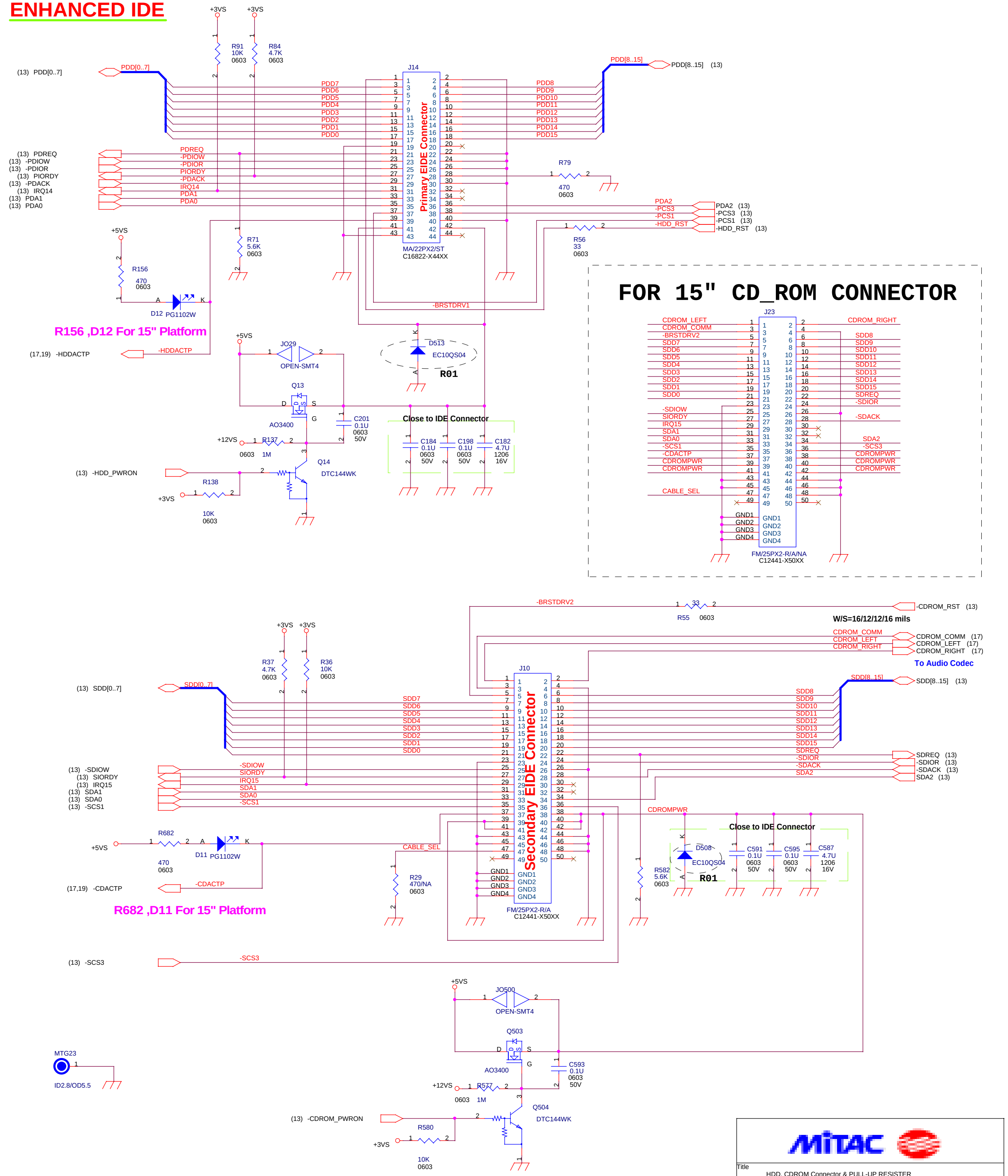


ISA BUS



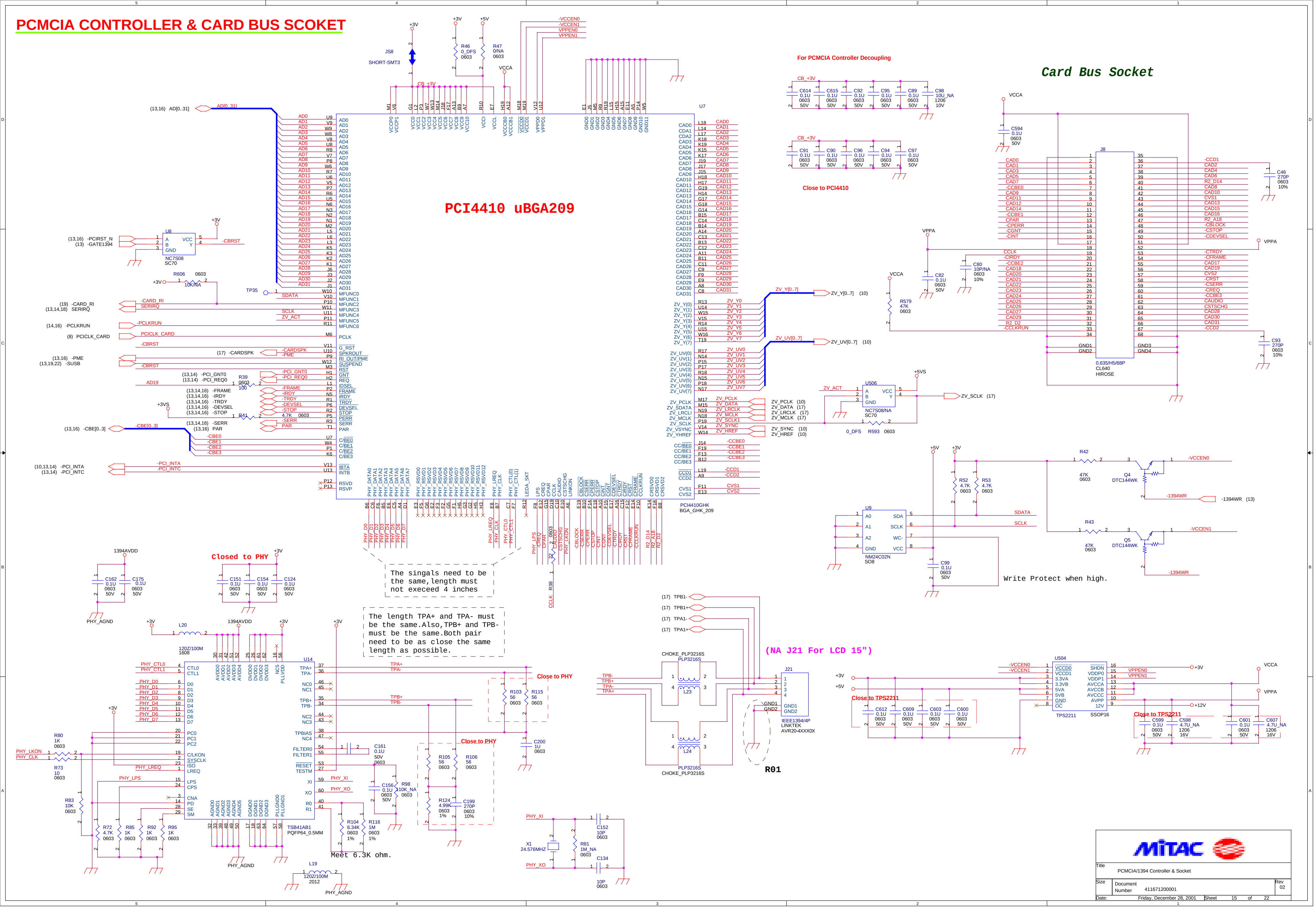
R01

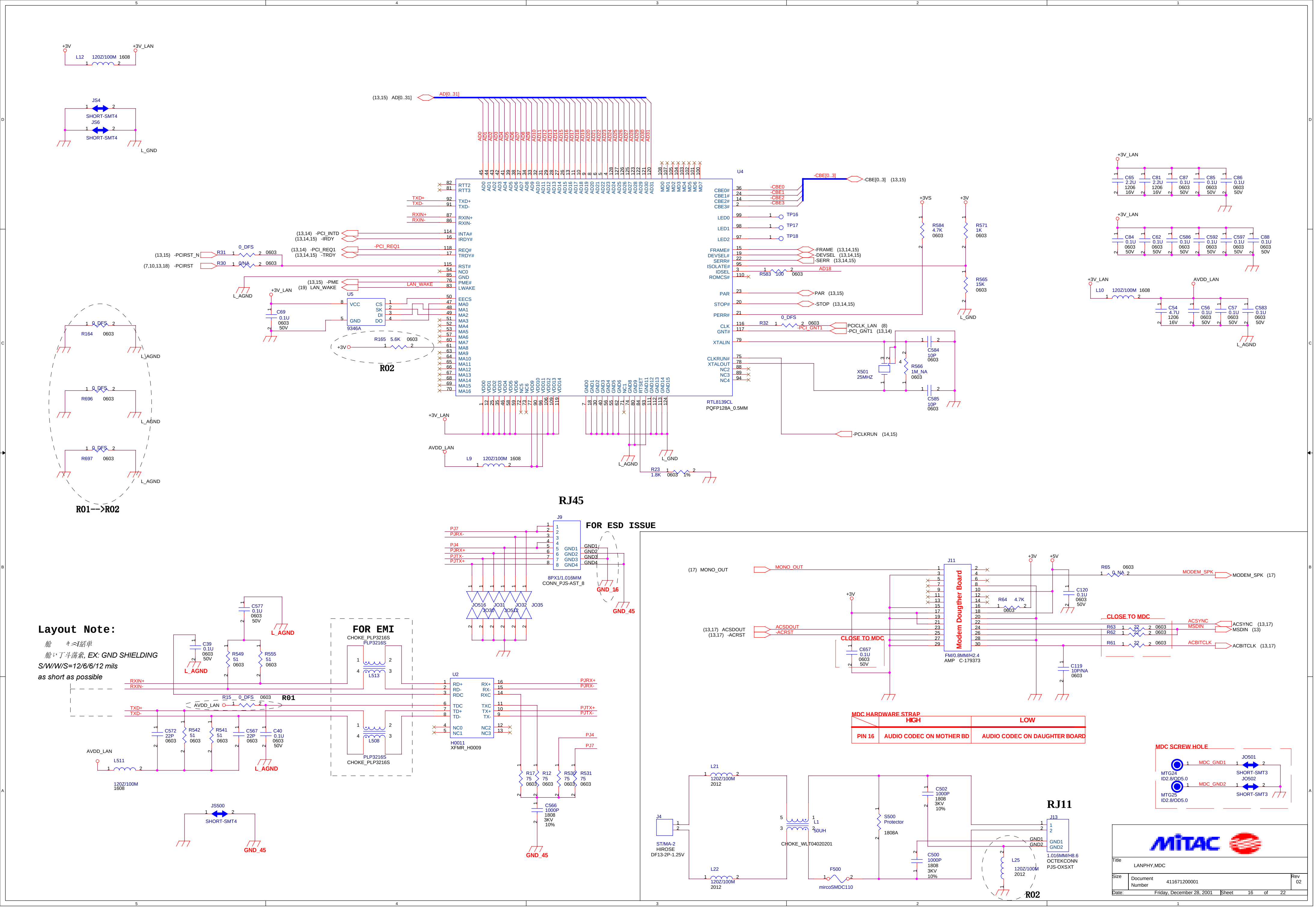
ENHANCED IDE



MiTAC

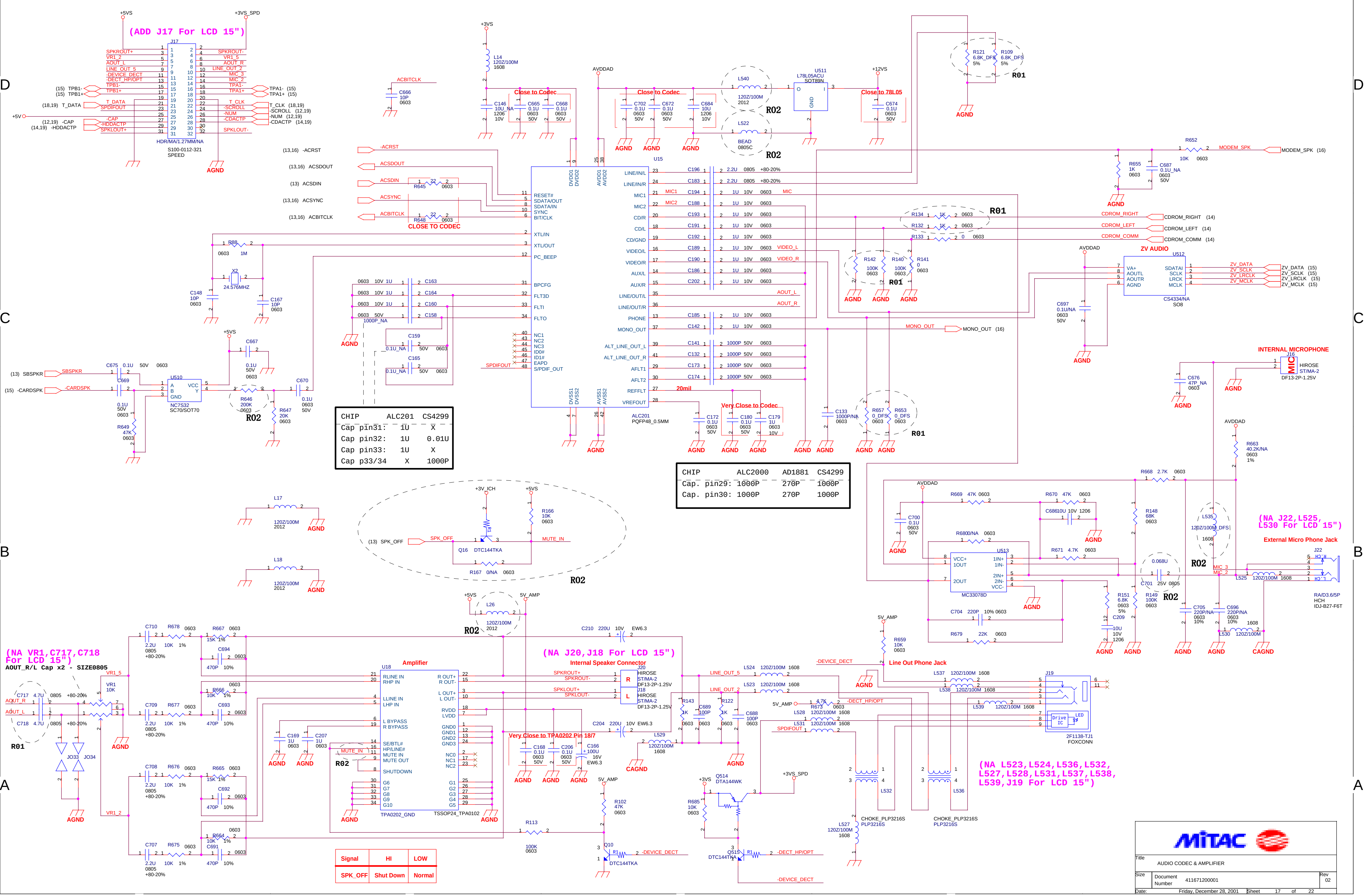
Title	HDD, CDROM Connector & PULL-UP RESISTER	
Size C	Document Number 411671200001	Rev 02
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PCMCIA CONTROLLER & CARD BUS SCOKET
PCI4410 uBGA209
Card Bus Socket
For PCMCIA Controller Decoupling
Close to PCI4410
Closed to PHY
The singals need to be the same,length must not execeed 4 inches
The length TPA+ and TPA- must be the same.Also,TPB+ and TPB- must be the same.Both pair need to be as close the same length as possible.
Close to PHY
Meet 6.3K ohm.
(NA J21 For LCD 15")
Close to TPS2211
Write Protect when high.
U7
PCI4410GHK
BGA_GHK_209
J8
CL640
HIROSE
U14
TSB41AB1
PQFP64_0.5MM
J21
IEEE1394/4P
LINKTEK
AVR20-4XXX0X
U504
TPS2211
SSOP16
U9
NM24C02N
SO8
U8
NC7S08
SC70
U506
NC7S08/NA
SC70
R01
MiTAC
Title
PCMCIA/1394 Controller & Socket
Size
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22



+3V
+3V_LAN
L12 120Z/100M 1608
JS4 SHORT-SMT4
JS6 SHORT-SMT4
L_GND
(13,15) AD[0..31]
AD[0..31]
U4
RTL8139CL
PQFP128A_0.5MM
-CBE[0..3]
CBE[0..3] (13,15)
U5
9346A
R165 5.6K 0603
R02
R01-->R02
(13,15) -PCIRST_N
(7,10,13,18) -PCIRST
(13,14) -PCI_INTD
(13,14,15) -IRDY
(13,14) -PCI_REQ1
(13,14,15) -TRDY
(13,15) -PME
(19) LAN_WAKE
-FRAME (13,14,15)
-DEVSEL (13,14,15)
-SERR (13,14,15)
-PAR (13,15)
-STOP (13,14,15)
PCICLK_LAN (8)
-PCI_GNT1 (13,14)
-PCLKRUN (14,15)
X501 25MHZ
+3VS
+3V_LAN
AVDD_LAN
L9 120Z/100M 1608
L10 120Z/100M 1608
R23 1.8K 0603 1%
L_AGND
RJ45
J9
8PX1/1.016MM
CONN_PJS-AST_8
FOR ESD ISSUE
GND_16
GND_45
FOR EMI
CHOKE_PLP3216S
L513
L508
U2
H0011
XFMR_H0009
Layout Note:
EX: GND SHIELDING
S/W/W/S=12/6/6/12 mils
as short as possible
RXIN+
RXIN-
TXD+
TXD-
PJRX+
PJRX-
PJTX+
PJTX-
PJ4
PJ7
R01
L511 120Z/100M 1608
JS500 SHORT-SMT4
C566 1000P 1808 3KV 10%
(17) MONO_OUT
MONO_OUT
J11
Modem Dougther Board
FM/0.8MM/H2.4
AMP C-179373
(13,17) ACSDOUT
(13,17) -ACRST
CLOSE TO MDC
MODEM_SPK (17)
ACSYNC (13,17)
MSDIN (13)
ACBITCLK (13,17)
MDC HARDWARE STRAP
| | HIGH | LOW |
| PIN 16 | AUDIO CODEC ON MOTHER BD | AUDIO CODEC ON DAUGHTER BOARD |
MDC SCREW HOLE
MTG24 ID2.8/OD5.0
MTG25 ID2.8/OD5.0
JO501 SHORT-SMT3
JO502 SHORT-SMT3
MDC_GND1
MDC_GND2
RJ11
J4
ST/MA-2
HIROSE
DF13-2P-1.25V
L21 120Z/100M 2012
L22 120Z/100M 2012
L1 50UH
CHOKE_WLT04020201
S500 Protector 1808A
F500 mircoSMDC110
C502 1000P 1808 3KV 10%
C500 1000P 1808 3KV 10%
J13
1.016MM/H8.6
OCTEKCONN
PJS-OXSXT
L25 120Z/100M 2012
R02
Title
LANPHY,MDC
Size
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02
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AUDIO CODE & AMPLIFIER



CHIP	ALC201	CS4299
Cap pin31:	1U	X
Cap pin32:	1U	0.01U
Cap pin33:	1U	X
Cap p33/34	X	1000P

CHIP	ALC2000	AD1881	CS4299
Cap. pin29:	1000P	270P	1000P
Cap. pin30:	1000P	270P	1000P

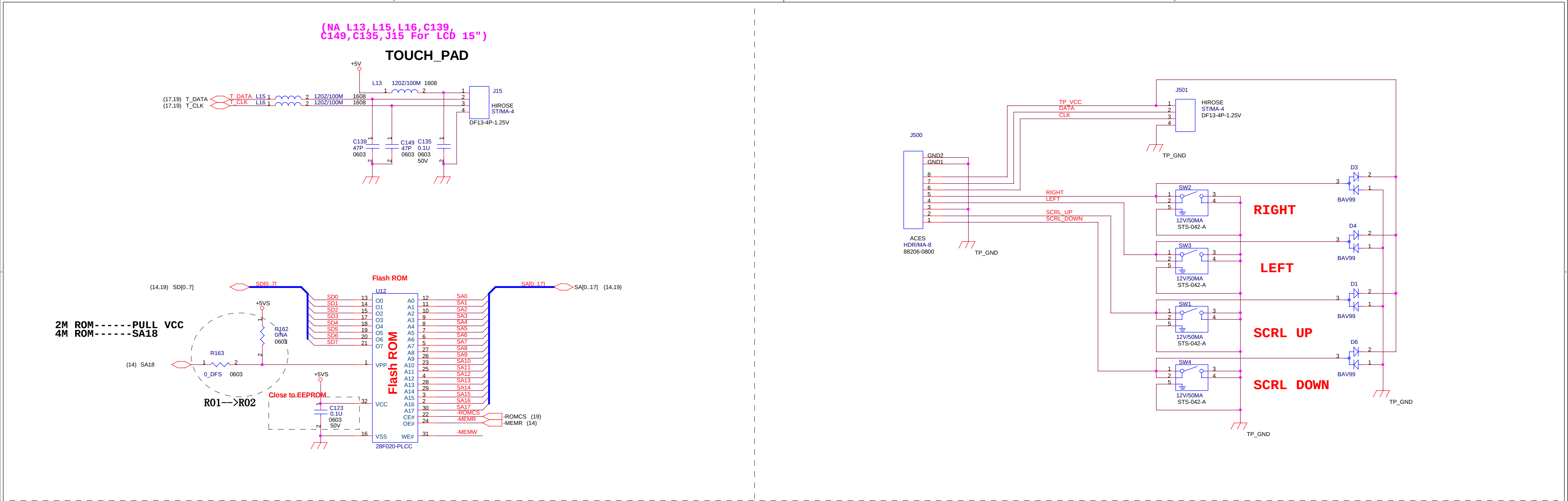
Signal	HI	LOW
SPK_OFF	Shut Down	Normal

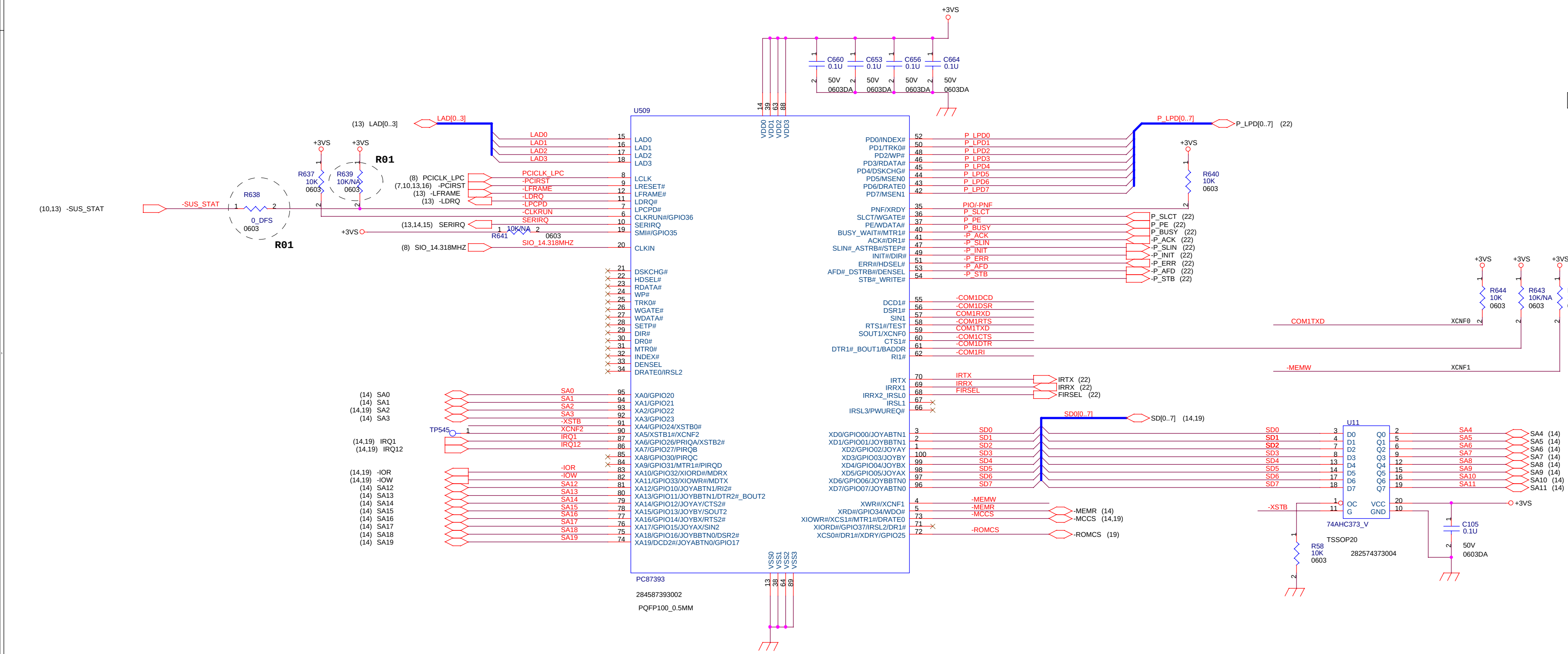
MiTAC

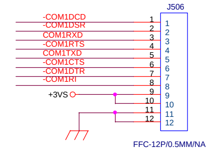
Title: AUDIO CODEC & AMPLIFIER

Size | Document Number: 411671200001 | Rev: 02

Date: Friday, December 28, 2001 | Sheet 17 of 22







STRAP OPTION

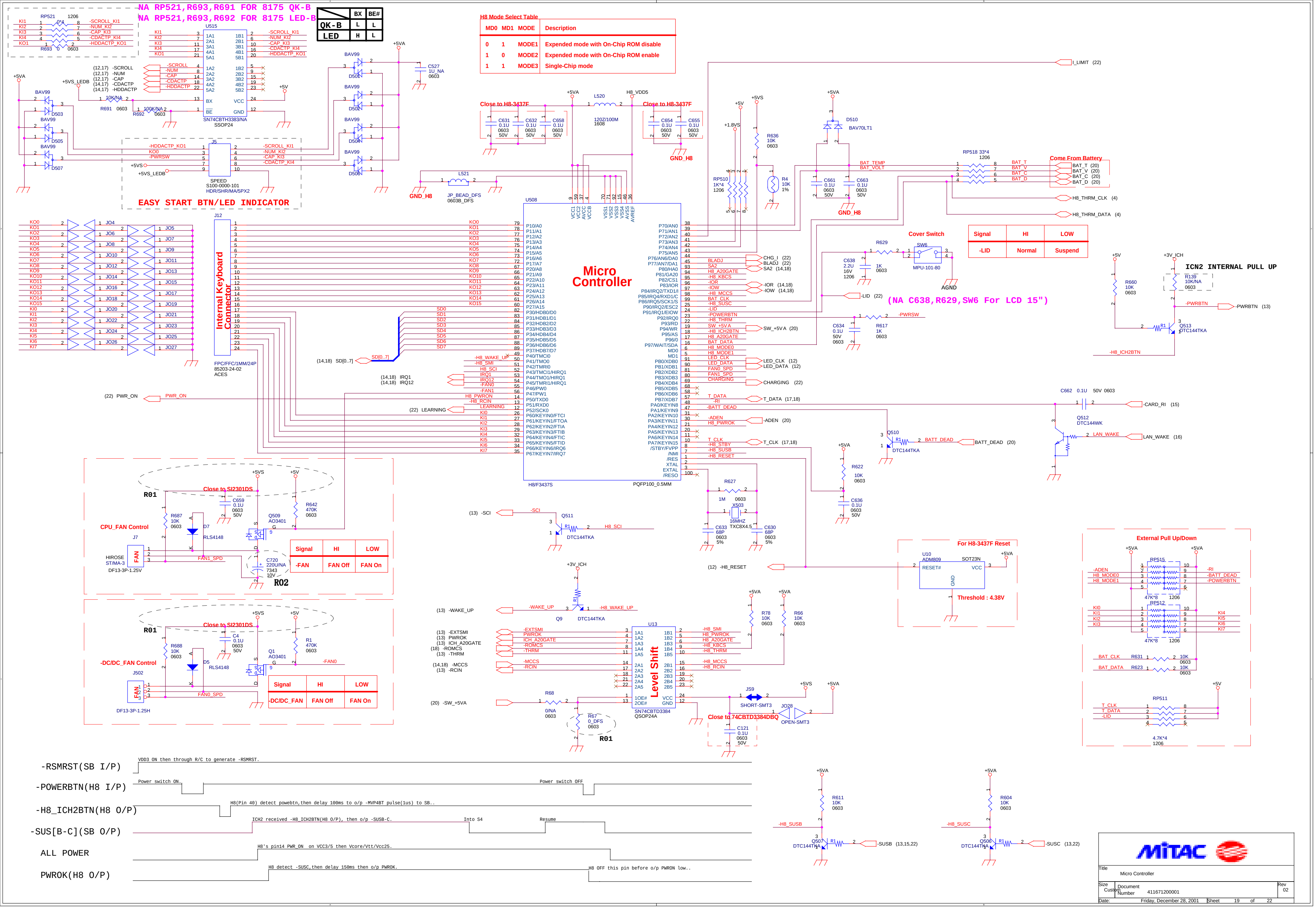
XCNF2	XCNF1	XCNF0	FUNCTIONALITY
X	0	0	NO BIOS
X	0	1	NORMAL MODE , XRDY DISABLE
0	1	0	LATCH MODE ,XA12-19, XRDY ENABLE
1	1	0	LATCH MODE , GPIO 10-17 , XRDY ENABLE
0	1	1	LATCH MODE , XA12-19, XRDY DISABLE
1	1	1	LATCH MODE , GPIO 10-17 ,XRDY DISABLE

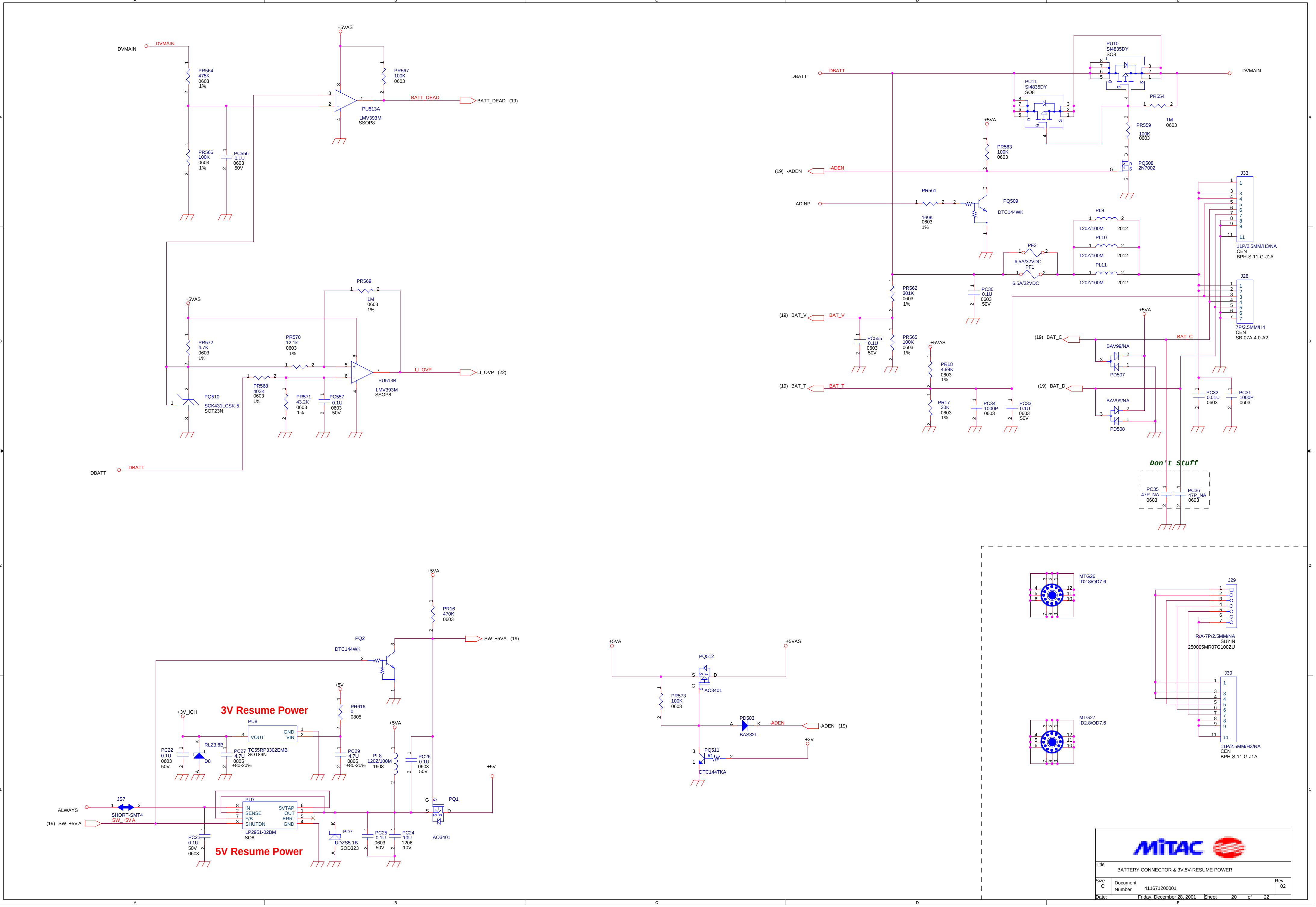
BASE ADDRESS SELECT

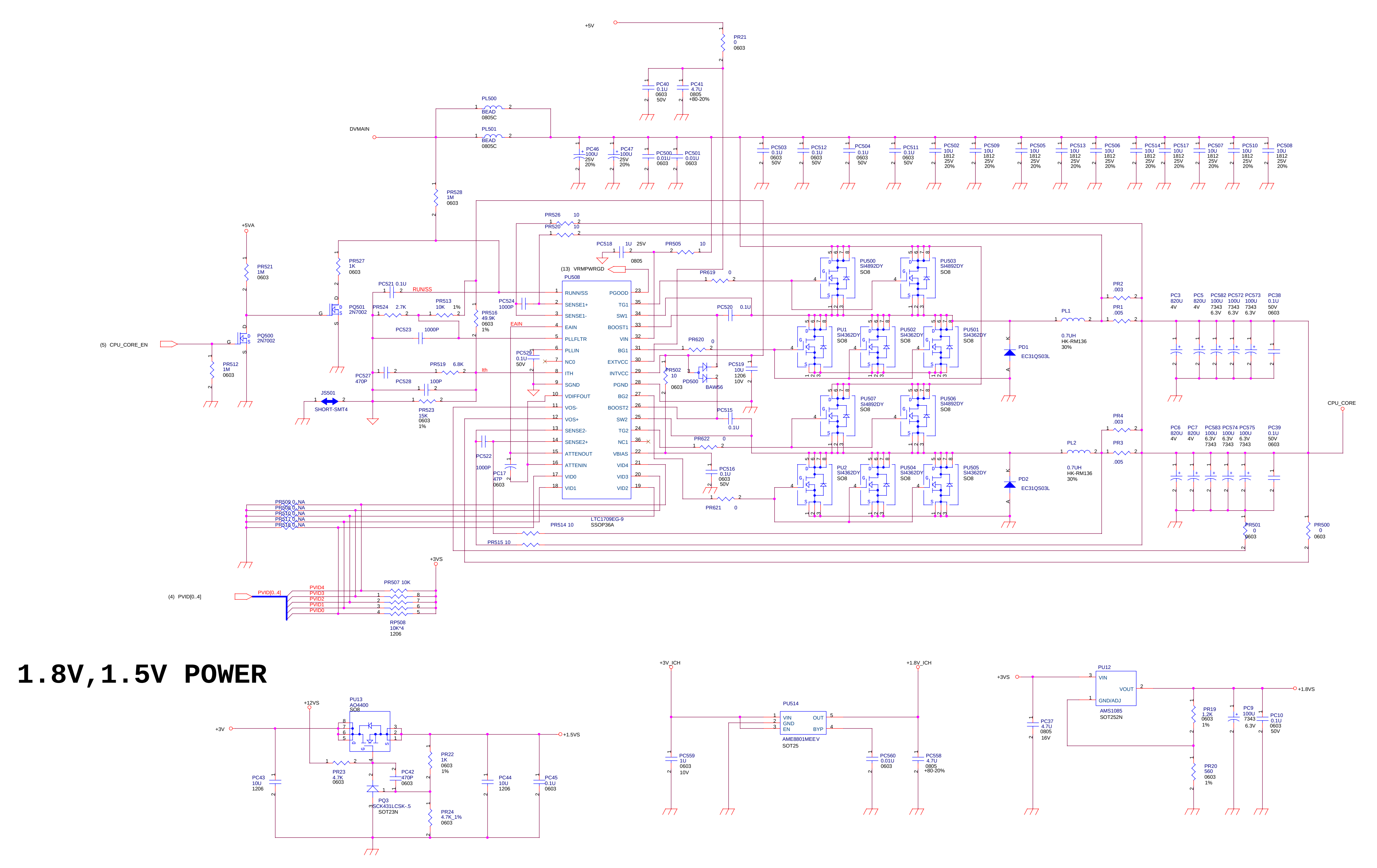
R303	INDEX REGISTER	DATA REGISTER
MOUNTED	4EH	4FH
OPEN	2EH	2FH

MITAC INTERNATIONAL CORP.

Title	TOUCH PAD,BIOS,SUPER-IO	
Size: Custom	Document Number: 411671200001	Rev: 02
Date: Friday, December 28, 2001	Sheet 18 of 22	

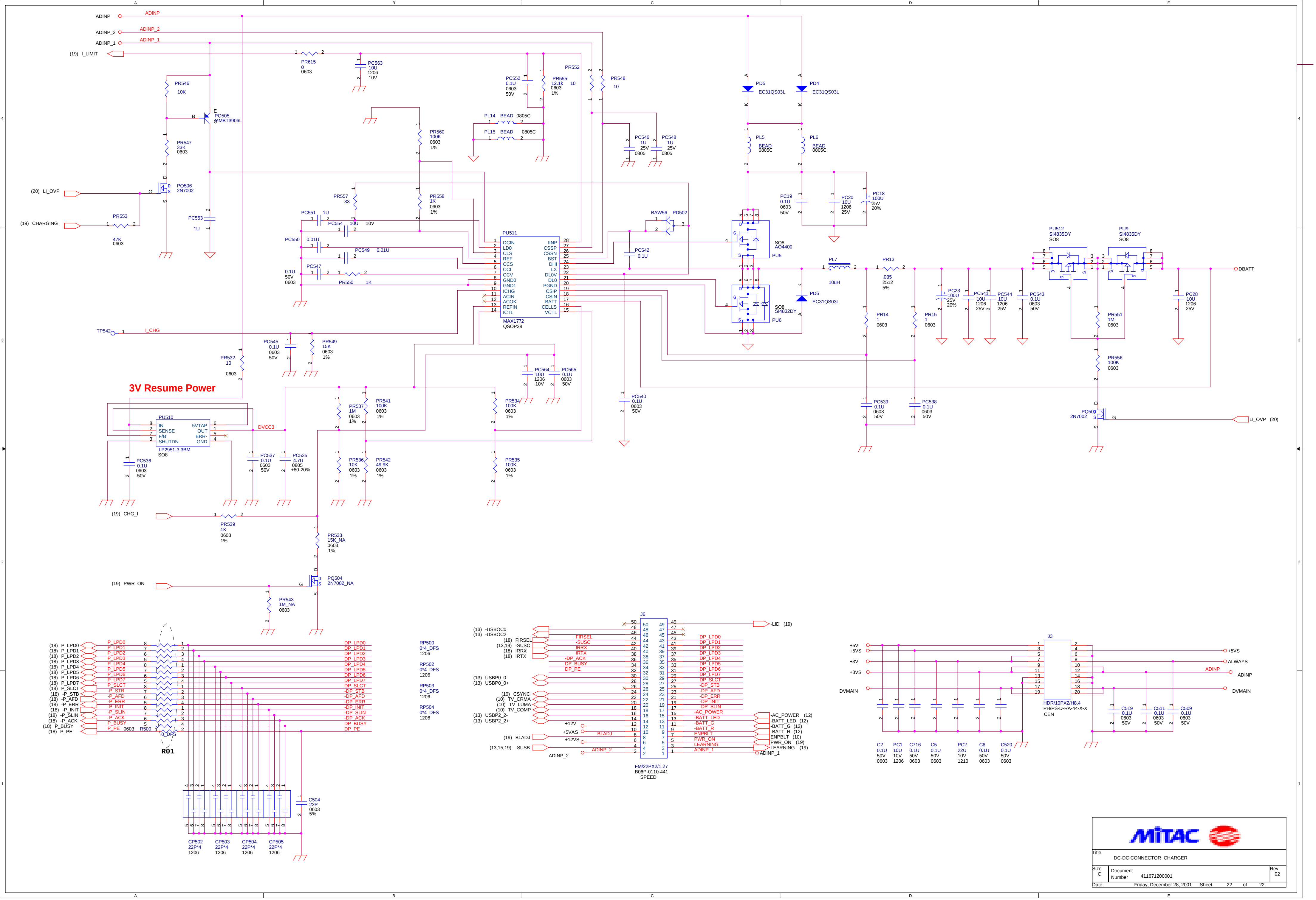

NA RP521,R693,R691 FOR 8175 QK-B
NA RP521,R693,R692 FOR 8175 LED-B
QK-B
LED
BX
BE#
H8 Mode Select Table
MD0 MD1 MODE Description
0 1 MODE1 Expended mode with On-Chip ROM disable
1 0 MODE2 Expended mode with On-Chip ROM enable
1 1 MODE3 Single-Chip mode
SN74CBTH3383/NA
SSOP24
Close to H8-3437F
EASY START BTN/LED INDICATOR
Internal Keyboard Connector
FPC/FFC/1MM/24P
85203-24-02
ACES
Micro Controller
H8/F3437S
PQFP100_0.5MM
Come From Battery
Cover Switch
MPU-101-80
Signal HI LOW
-LID Normal Suspend
ICN2 INTERNAL PULL UP
(NA C638,R629,SW6 For LCD 15")
CPU_FAN Control
Close to SI2301DS
Signal HI LOW
-FAN FAN Off FAN On
-DC/DC_FAN Control
Signal HI LOW
-DC/DC_FAN FAN Off FAN On
For H8-3437F Reset
ADM809
Threshold : 4.38V
External Pull Up/Down
Level Shift
SN74CBTD3384
QSOP24A
Close to 74CBTD3384DBQ
-RSMRST(SB I/P)
VDD3 ON then through R/C to generate -RSMRST.
-POWERBTN(H8 I/P)
Power switch ON.
Power switch OFF
-H8_ICH2BTN(H8 O/P)
H8(Pin 40) detect powebtn,then delay 100ms to o/p -MVP4BT pulse(1us) to SB..
-SUS[B-C](SB O/P)
ICH2 received -H8_ICH2BTN(H8 O/P), then o/p -SUSB-C.
Into S4
Resume
ALL POWER
H8's pin14 PWR_ON on VCC3/5 then Vcore/Vtt/Vcc25.
PWROK(H8 O/P)
H8 detect -SUSC,then delay 150ms then o/p PWROK.
H8 OFF this pin before o/p PWRON low..
MiTAC
Title
Micro Controller
Size Custom
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DVMAIN
PR564 475K 0603 1%
PR566 100K 0603 1%
PC556 0.1U 0603 50V
+5VAS
PR567 100K 0603
PU513A LMV393M SSOP8
BATT_DEAD
BATT_DEAD (19)
PR569 1M 0603 1%
PR570 12.1k 0603 1%
PR572 4.7K 0603 1%
PR568 402K 0603 1%
PR571 43.2K 0603 1%
PC557 0.1U 0603 50V
PU513B LMV393M SSOP8
LI_OVP
LI_OVP (22)
PQ510 SCK431LCSK-5 SOT23N
DBATT
PU10 SI4835DY SO8
PU11 SI4835DY SO8
PR554 1M 0603
PR559 100K 0603
PQ508 2N7002
PR563 100K 0603
+5VA
(19) -ADEN
-ADEN
ADINP
PR561 169K 0603 1%
PQ509 DTC144WK
PL9 120Z/100M 2012
PL10 120Z/100M 2012
PL11 120Z/100M 2012
PF2 6.5A/32VDC
PF1 6.5A/32VDC
J33 11P/2.5MM/H3/NA CEN BPH-S-11-G-J1A
J28 7P/2.5MM/H4 CEN SB-07A-4.0-A2
PR562 301K 0603 1%
PC30 0.1U 0603 50V
(19) BAT_V
BAT_V
PC555 0.1U 0603 50V
PR565 100K 0603 1%
PR18 4.99K 0603 1%
PR17 20K 0603 1%
(19) BAT_T
BAT_T
PC34 1000P 0603
PC33 0.1U 0603 50V
(19) BAT_C
BAT_C
BAV99/NA
PD507
(19) BAT_D
PD508
PC32 0.01U 0603
PC31 1000P 0603
Don't Stuff
PC35 47P_NA 0603
PC36 47P_NA 0603
MTG26 ID2.8/OD7.6
MTG27 ID2.8/OD7.6
J29 R/A-7P/2.5MM/NA SUYIN 250005MR07G100ZU
J30 11P/2.5MM/H3/NA CEN BPH-S-11-G-J1A
PR16 470K 0603
PQ2 DTC144WK
-SW_+5VA (19)
+5V
PR616 0 0805
3V Resume Power
+3V_ICH
PU8 TC55RP3302EMB SOT89N
VOUT GND VIN
PC22 0.1U 0603 50V
RLZ3.6B D8
PC27 4.7U 0805 +80-20%
PC29 4.7U 0805 +80-20%
PL8 120Z/100M 1608
PC26 0.1U 0603 50V
ALWAYS
JS7 SHORT-SMT4
(19) SW_+5VA
SW_+5VA
PU7 LP2951-02BM SO8
IN SENSE F/B SHUTDN 5VTAP OUT ERR- GND
PC21 0.1U 50V 0603
5V Resume Power
PD7 UDZS5.1B SOD323
PC25 0.1U 0603 50V
PC24 10U 1206 10V
PQ1 AO3401
PQ512 AO3401
PR573 100K 0603
PD503 BAS32L
-ADEN (19)
+3V
PQ511 DTC144TKA
MiTAC
Title BATTERY CONNECTOR & 3V,5V-RESUME POWER
Size C
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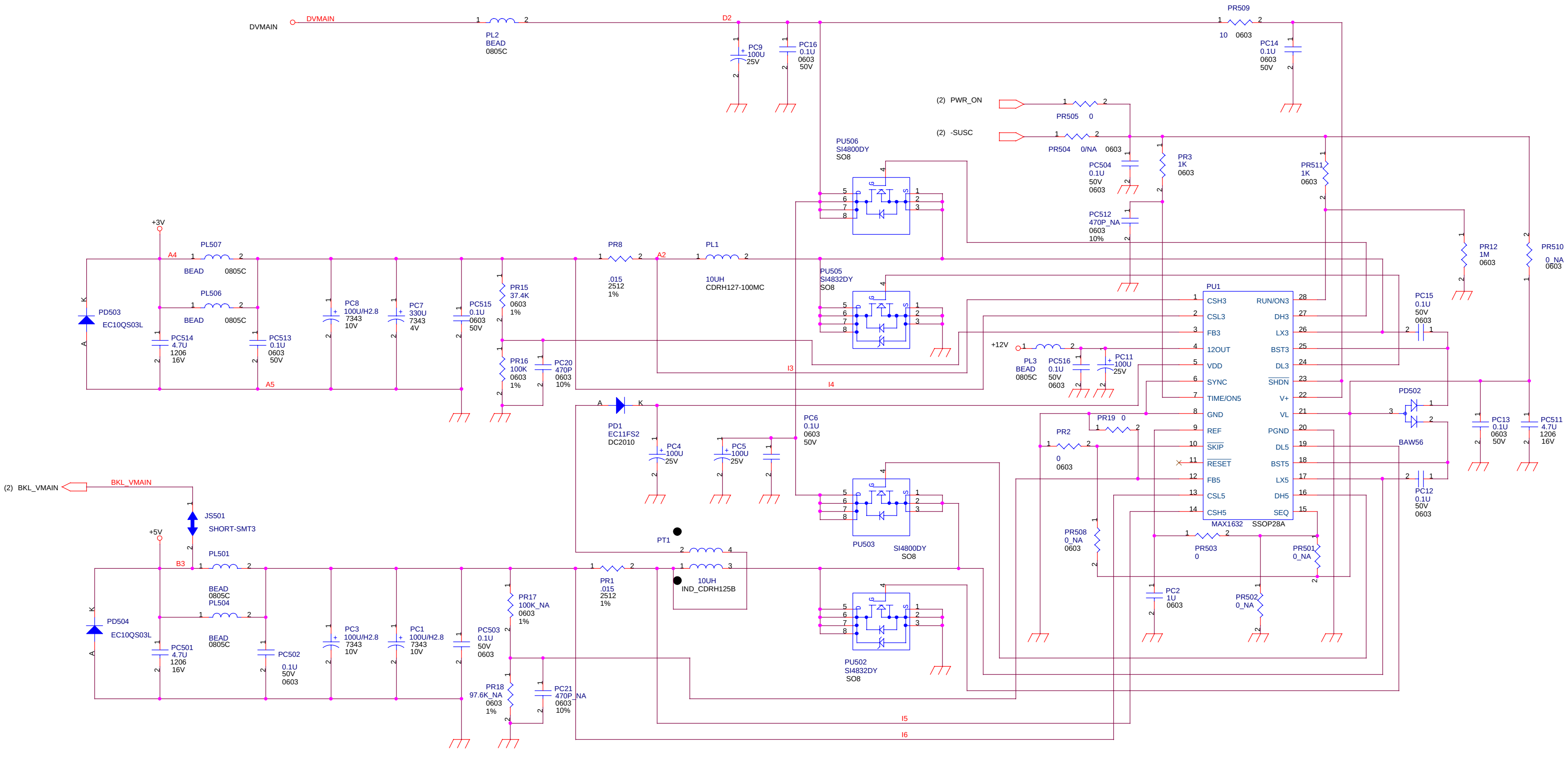


1.8V,1.5V POWER

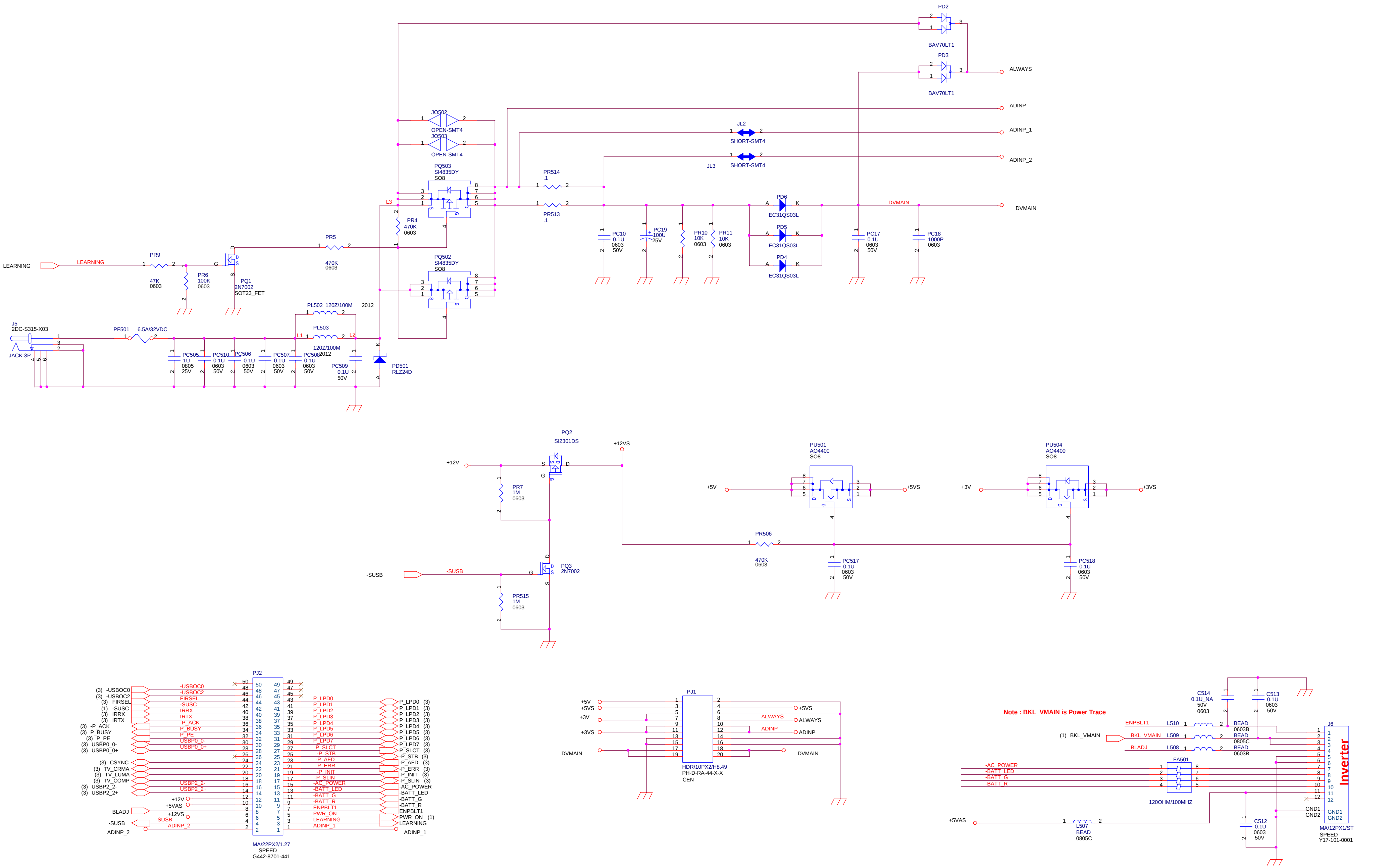
Title	CPU Vcore/VTT
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3V Resume Power
MAX1772
QSOP28
PU511
LP2951-3.3BM
PU510
R01
J6
J3
DBATT
ADINP
ADINP_2
ADINP_1
I_LIMIT
LI_OVP
CHARGING
I_CHG
CHG_I
PWR_ON
DVCC3
Title
DC-DC CONNECTOR ,CHARGER
Size C
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SYSTEM POWER (5V 3V 12V)



Title	SYSTEM POWER	
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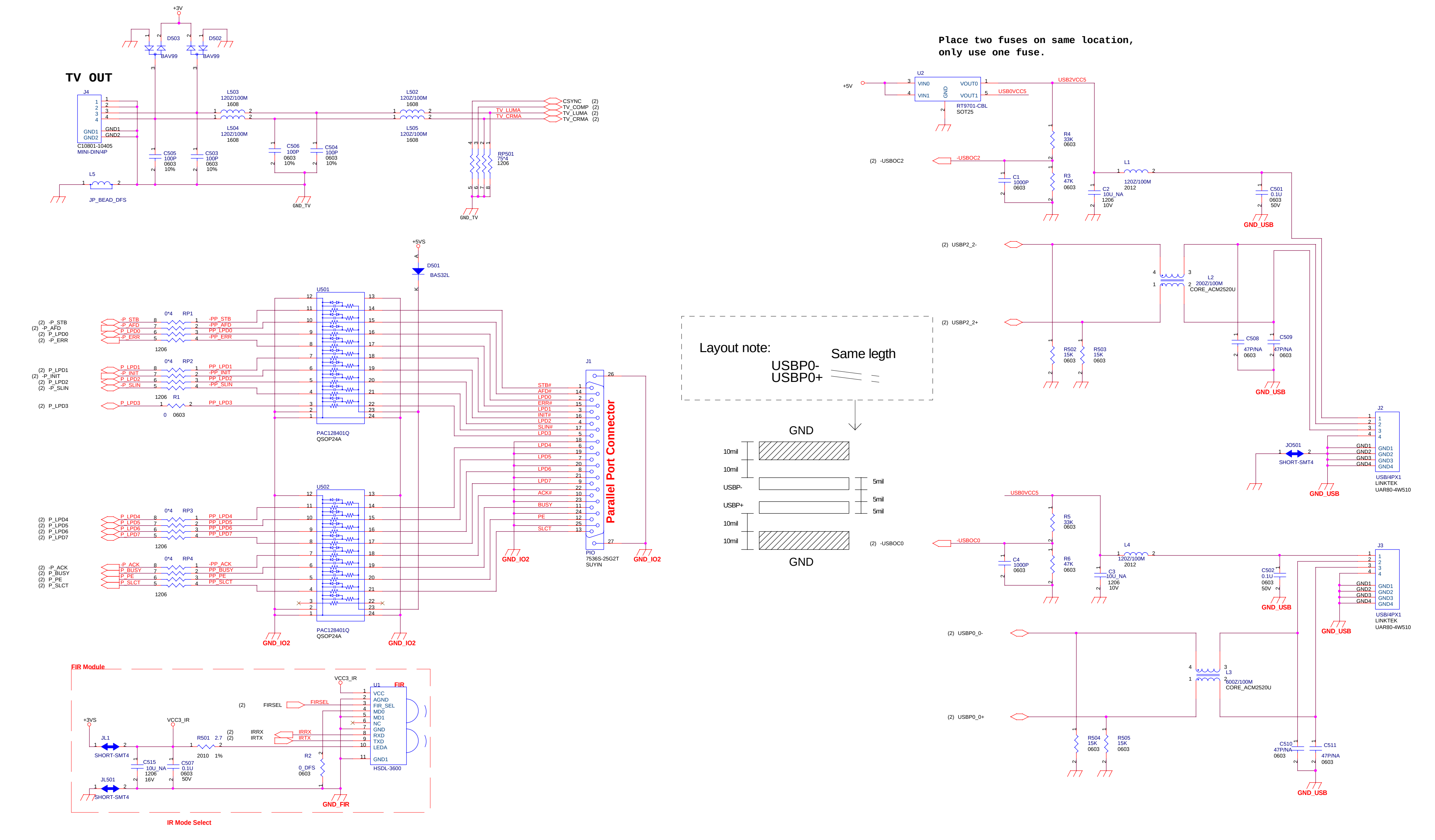


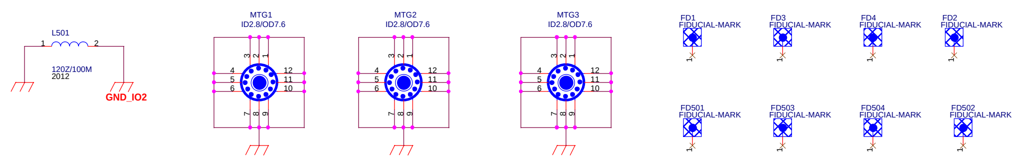
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Title: DC POWER

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IR Mode Select

IRMODE0	IRMODE1	FIRSEL	RX Function	TX Function
HI	LOW	X	Shutdown	Shutdown
LOW	LOW	LOW		Full Distance Power
LOW	HI	LOW	SIR	2/3 Distance Power
HI	HI	LOW	SIR	1/3 Distance Power
LOW	LOW	HI	MIR/FIR	Full Distance Power
LOW	HI	HI	MIR/FIR	2/3 Distance Power
HI	HI	HI	MIR/FIR	1/3 Distance Power

Title	DC POWER
Size	
Document Number	411671200004
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Reference Material

- **Intel Pentium 4 Processor mFC-PGA2 478Pin** .... ***Intel. INC***
- **INTEL 82845 Memory Controller Hub** .... ***Intel. INC***
- **INTEL 82801BA I/O Controller Hub** .... ***Intel. INC***
- **PCI4410 Manual-PC Card and OHCI Controller** .... ***CHRONTEL. INC***
- **Frequency Generator ICS950805** .... ***ICS. INC***
- **Engineer Hardware Specification** .... ***Technology.Corp/MiTAC***
- **Engineer Software Specification** .... ***Technology.Corp/MiTAC***

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